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1 Introduction to the SPI515 Adjustable Voltage Parallel Port JTAG Emulator .......... 1-1
Provides an overview of the SPI515 along with the keys features.
1.0 Overview of the SPI515 ........................................... 1-2
1.1 Key Features of the SPI515 ....................................... 1-2
1.2 Key Items on the SPI515 ......................................... 1-3
2 Installing the SPI515 Adjustable Voltage Parallel Port JTAG Emulator .......... 2-1
Lists the hardware and software you'll need to install the SPI515 Adjustable Voltage Parallel Port JTAG Emulator, and the installation procedure of the SPI515 in your system.
2.1 What You'll Need .................................................. 2-2
   Hardware checklist .................................................. 2-2
   Software checklist .................................................. 2-2
2.2 Voltage Selection .................................................. 2-3
2.3 Installing the SPI515 Adjustable Voltage Parallel Port JTAG Emulator .......... 2-4
2.3.1 SPI515 Installation Checklist .................................. 2-4
2.4 SPI515 LEDs ....................................................... 2-6
2.5 WAIT-IN-RESET .................................................... 2-6
3 Specifications For Your Target System's Connection to the Emulator .......... 4-1
Contains information about connecting your target system to the SPI515 Adjustable Voltage Parallel Port JTAG Emulator
3.1 Designing Your Target System's Emulator Connector (14-pin Header) .......... 3-2
3.2 Bus Protocol ...................................................... 3-3
3.3 Emulator Cable Pod Logic ......................................... 3-4
3.4 Emulator Cable Pod Signal Timing ................................ 3-5
3.5 Buffering Signals Between the Emulator and the Target System .......... 3-6
3.6 Emulation Timing Calculations .................................. 3-9
3.7 Mechanical Dimensions of the SPI515 Adjustable Voltage JTAG Emulator .... 3-11
4 Specifications For Your Target's I/O Interface to the Emulator .......... 4-1
Contains information about connecting your target system's logging interface to the SPI515 Adjustable Voltage Parallel Port JTAG Emulator
4.1 Designing Your Target System's Logging Connector .......................... 4-2
4.2 Data Logging Signal Timing ....................................... 4-3
4.3 Data Logging Circuitry .............................................. 4-3
4.4 Data Logging Connections .......................................... 4-4
About This Manual

This document describes the module level operations of the SPI515 Adjustable Voltage Parallel Port JTAG Emulator. This emulator is designed to be used with digital signal processors (DSPs) and microcontrollers designed by Texas Instruments.

The SPI515 Adjustable Voltage Parallel Port JTAG Emulator is a tabletop module that attaches to a personal computer or laptop to allow hardware engineers and software programmers to develop applications with DSPs and microcontrollers.

Notational Conventions

This document uses the following conventions.

The SPI515 Adjustable Voltage Parallel Port JTAG Emulator will sometimes be referred to as the SPI515.

Program listings, program examples, and interactive displays are shown in a special italic typeface. Here is a sample program listing.

\[ \text{equations} \]
\[ \text{lrd} = \text{lstrobe\&rw}; \]

Information About Cautions

This book may contain cautions.

\textit{This is an example of a caution statement.}

A caution statement describes a situation that could potentially damage your software, or hardware, or other equipment. The information in a caution is provided for your protection. Please read each caution carefully.

Related Documents

Texas Instruments Code Composer Users Guide
Texas Instruments High Level Language Debugger Users Guide
Chapter 1

Introduction to the SPI515 Adjustable Voltage Parallel Port JTAG Emulator

This chapter provides you with a description of the SPI515 Adjustable Voltage Parallel Port JTAG Emulator along with the key features.

<table>
<thead>
<tr>
<th>Topic</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0 Overview of the SPI515</td>
<td>1-2</td>
</tr>
<tr>
<td>1.1 Key Features of the SPI515</td>
<td>1-2</td>
</tr>
<tr>
<td>1.2 Key Items on the SPI515</td>
<td>1-3</td>
</tr>
</tbody>
</table>
1.0 Overview of the SPI515

The SPI515 Adjustable Voltage Parallel Port JTAG Emulator is designed to be used with digital signal processors (DSPs) and microprocessors which operate between +0.8 volts to +5 volts. This emulator is powered from an external power supply which is included with the emulator. This means no power is drawn from the target system.

The SPI515 emulator automatically adjusts to the voltage level of the logic that it will be controlling.

The SPI515 is designed to be compatible with the existing Texas Instruments XDS510 emulator and operate with debuggers provided by Texas Instruments.

1.1 Key Features of the SPI515

The SPI515 Adjustable Voltage Parallel Port JTAG Emulator has the following features:

• Supports Texas Instrument's Digital Signal Processors and Microcontrollers with JTAG interface (IEEE 1149.1)

• Compatible with Texas Instrument's XDS510 emulator.

• Advanced emulation controller provides high performance.

• Supports standard parallel communication interface with host PC (SPP8, EPP, and ECP). No adapter required.

• Supports JTAG interfaces from 1-5 volts.

• Six status LEDs for operational status.

• Incorporates EMU0/EMU1 Wait-In-Reset features for TMS27xx DSPs.

• High speed data logging support over EMU0/1 pins.

• 4 bits of user programmable I/O with variable voltage.

• Power provided by supplied power supply.

• Supports the Texas Instruments Code High Level Language ‘C’ Debugger

• Compatible with Texas Instruments Code Composer Studio
1.2 Key Items on the SPI515

Figure 1-1 shows the SPI515. The key items identified are:

- Status LEDs
- JTAG connector
- Tail
- Programmable I/O interface
- DB-25 connector to the host adapter card
- Power connector
This chapter helps you install the SPI515 Adjustable Voltage Parallel Port JTAG Emulator. For use with specific software packages such as the Code Composer Studio or TI HLL debugger refer to their respective documentation.

<table>
<thead>
<tr>
<th>Topic</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.1 What You’ll Need</td>
<td>2-2</td>
</tr>
<tr>
<td>Hardware checklist</td>
<td>2-2</td>
</tr>
<tr>
<td>Software checklist</td>
<td>2-2</td>
</tr>
<tr>
<td>2.2 Voltage Selection</td>
<td>2-3</td>
</tr>
<tr>
<td>2.3 Installing the SPI515 Adjustable Voltage Parallel Port JTAG Emulator</td>
<td>2-4</td>
</tr>
<tr>
<td>2.3.1 SPI515 Installation Checklist</td>
<td>2-4</td>
</tr>
<tr>
<td>2.4 SPI515 LEDs</td>
<td>2-6</td>
</tr>
<tr>
<td>2.5 WAIT-IN-RESET</td>
<td>2-6</td>
</tr>
</tbody>
</table>
2.1 What You’ll Need

The following checklists detail items that are shipped with the SPI515 and additional items you’ll need to use these tools.

**Hardware checklist**

- **host** An IBM PC/AT or 100% compatible PC or laptop with a hard-disk system and a 1.44M floppy-disk drive with SPP8, EPP, or ECP compatible parallel port
- **memory** Minimum of 32MB
- **display** Color VGA or LCD
- **emulator module** SPI515 Adjustable Voltage Parallel Port JTAG emulator with power supply
- **target system** A board with a TI DSP or Microcontroller and power supply
- **connector to target system** 14-pin connector (two rows of seven pins) --- see Chapter 3 for more information about this connector

**Software checklist**

- **operating system** Win 95, Win 98, or Win NT 4.0
- **software tools** Compiler/assembler/linker for DSP or Microcontroller
- **debugger** Code Composer Studio or TI HLL Debugger
- **drivers** drivers for TI Code Composer

\* Included as part of the SPI515 package
2.2 Voltage Selection

The SPI515 automatically adjusts to the voltage level of the logic that it will be controlling. Table 1 below shows the 18 input and output voltage levels, and target system voltages that will be used. There will be some range overlap due to cable length, noise, etc.

The Signal Output Voltage is the voltage level on the TMS, TDI, TCK, and TRST pins.

The Signal Input Threshold is the voltage level on the TCK_RET, TDO, EMU0, and EMU1 pins.

**WARNING !**

The Power Detect Input Threshold is the voltage level on the PD pin.

<table>
<thead>
<tr>
<th>Signal Output Voltage</th>
<th>Power Detect Threshold</th>
<th>Signal Input JTAG Threshold</th>
<th>Target System Voltage (PD Pin)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.900</td>
<td>0.540</td>
<td>0.540</td>
<td>0.83 - 0.97</td>
</tr>
<tr>
<td>1.000</td>
<td>0.600</td>
<td>0.570</td>
<td>0.93 - 1.07</td>
</tr>
<tr>
<td>1.100</td>
<td>0.660</td>
<td>0.630</td>
<td>1.03 - 1.17</td>
</tr>
<tr>
<td>1.200</td>
<td>0.720</td>
<td>0.660</td>
<td>1.13 - 1.27</td>
</tr>
<tr>
<td>1.300</td>
<td>0.780</td>
<td>0.710</td>
<td>1.23 - 1.37</td>
</tr>
<tr>
<td>1.400</td>
<td>0.840</td>
<td>0.730</td>
<td>1.33 - 1.47</td>
</tr>
<tr>
<td>1.500</td>
<td>0.900</td>
<td>0.780</td>
<td>1.43 - 1.57</td>
</tr>
<tr>
<td>1.600</td>
<td>0.960</td>
<td>0.800</td>
<td>1.53 - 1.67</td>
</tr>
<tr>
<td>1.700</td>
<td>1.020</td>
<td>0.850</td>
<td>1.63 - 1.77</td>
</tr>
<tr>
<td>1.800</td>
<td>1.080</td>
<td>0.900</td>
<td>1.73 - 1.87</td>
</tr>
<tr>
<td>1.900</td>
<td>1.140</td>
<td>0.950</td>
<td>1.83 - 1.97</td>
</tr>
<tr>
<td>2.000</td>
<td>1.200</td>
<td>1.000</td>
<td>1.93 - 2.07</td>
</tr>
<tr>
<td>2.200</td>
<td>1.320</td>
<td>1.100</td>
<td>2.13 - 2.27</td>
</tr>
<tr>
<td>2.400</td>
<td>1.440</td>
<td>1.200</td>
<td>2.33 - 2.47</td>
</tr>
<tr>
<td>2.600</td>
<td>1.560</td>
<td>1.300</td>
<td>2.53 - 2.67</td>
</tr>
<tr>
<td>2.800</td>
<td>1.680</td>
<td>1.400</td>
<td>2.73 - 2.87</td>
</tr>
<tr>
<td>3.000</td>
<td>1.800</td>
<td>1.500</td>
<td>2.93 - 3.07</td>
</tr>
<tr>
<td>3.200</td>
<td>1.920</td>
<td>1.600</td>
<td>3.13 - 5.00</td>
</tr>
</tbody>
</table>
2.3 Installing the SPI515 Adjustable Voltage Parallel Port JTAG Emulator

This section contains the steps for installing the SPI515 Adjustable Voltage Parallel Port JTAG Emulator.

### WARNING

Target Cable Connectors:

Be very careful with the target cable connectors. connect them gently; don’t force them into position, or you may damage the connectors.

Do **not** connect or disconnect the DB-25 connector while the PC is powered up.

Do **not** connect or disconnect the 14-pin cable while the target system is powered up.

#### 2.3.1 SPI515 Installation Checklist

To install the SPI515 execute the following checklist:

- Turn off the power to your PC or laptop
- Turn off the power to your target system (DSP or microcontroller system)
- Attach the SPI515 DB-25 connector to the parallel port on the PC or laptop with the supplied cable.
- Plug power supply for the SPI515 emulator into the emulator.
- Plug power supply for the SPI515 emulator into a 110/220 VAC outlet.
- Your system configuration should now look like that in Figure 2.1
- Apply power to your target.
- Apply power to your PC or laptop.
Figure 2-1 shows how you connect the SPI515 in a typical system configuration with a host PC and target board.
2.4 SPI515 LEDs

The SPI515 has 6 red Light Emitting Diodes (LEDs). These LEDs provide the user with the status of the emulator. The meaning of each LED is described in the table below.

Table 2: SPI515 LEDs

<table>
<thead>
<tr>
<th>LED Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>XMIT</td>
<td>Indicates data is being transmitted to the host system</td>
</tr>
<tr>
<td>RECV</td>
<td>Indicates data is being received from the host system</td>
</tr>
<tr>
<td>ST1</td>
<td>When on it indicates the TRSTn signal is low</td>
</tr>
<tr>
<td>ST0</td>
<td>When on indicates EMU0 signal is low (for WAIT-IN-RESET)</td>
</tr>
<tr>
<td>TPOWn</td>
<td>Indicates target power has dropped below input threshold</td>
</tr>
<tr>
<td>Power</td>
<td>Indicates power has been applied to the SPI515 emulator</td>
</tr>
</tbody>
</table>

2.5 WAIT-IN-RESET

Newer TI DSPs (e.g. TMS320C27x) have a feature called Wait-In-Reset. When the SPI515 detects the loss of target power it will drive EMU0 to 0 volts. When the target system is powered on and EMU0 = 0 volts, EMU1 = Vcc, and TRSTn = 0 volts then the DSP will wait in reset until the debugger is started. On processors that do not support Wait-In-Reset* pulling EMU0 should have no effect. EMU0 is tri-stated within 20 milliseconds after TRST returns high. A 100 ohm resistor is included in the event that the target system is driving this signal. Normally this signal is pulled high on the target system with a 4.7K ohm or larger resistor.
Chapter 3
Specifications For Your Target System’s Connection to the Emulator

This chapter contains information about connecting your target system to the emulator. Your target system must use a special 14-pin connector for proper communication with the emulator.

<table>
<thead>
<tr>
<th>Topic</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.1 Designing Your Target System’s Emulator Connector (14-pin Header)</td>
<td>3-2</td>
</tr>
<tr>
<td>3.2 Bus Protocol</td>
<td>3-3</td>
</tr>
<tr>
<td>3.3 Emulator Cable Pod Logic</td>
<td>3-4</td>
</tr>
<tr>
<td>3.4 Emulator Cable Pod Signal Timing</td>
<td>3-5</td>
</tr>
<tr>
<td>3.5 Buffering Signals Between the Emulator and the Target System</td>
<td>3-6</td>
</tr>
<tr>
<td>3.6 Emulation Timing Calculations</td>
<td>3-9</td>
</tr>
<tr>
<td>3.7 Mechanical Dimensions of the SPI515 Adjustable Voltage Scan Path Interface Pod</td>
<td>3-11</td>
</tr>
</tbody>
</table>
3.1 Designing Your Target System’s Emulator Connector (14-pin Header)

Certain devices support emulation through a dedicated emulation port. This port is a superset of the IEEE 1149.1 (JTAG) standard and is accessed by the emulator. To perform emulation with the emulator, your target system must have a 14-pin header (2 rows of 7 pins) with the connections that are shown in Figure 3-1. Table 1 describes the emulation signals.

Table 1: 14-Pin Header Signal Description

<table>
<thead>
<tr>
<th>Signal</th>
<th>Description</th>
<th>Emulator State</th>
<th>Target State</th>
</tr>
</thead>
<tbody>
<tr>
<td>TMS</td>
<td>JTAG test mode select.</td>
<td>Output</td>
<td>Input</td>
</tr>
<tr>
<td>TDI</td>
<td>JTAG test data input.</td>
<td>Output</td>
<td>Input</td>
</tr>
<tr>
<td>TDO</td>
<td>JTAG test data output.</td>
<td>Input</td>
<td>Output</td>
</tr>
<tr>
<td>TCK</td>
<td>JTAG test clock. TCK is a 10-MHz clock source from the emulation pod. This signal can be used to drive the system test clock.</td>
<td>Output</td>
<td>Input</td>
</tr>
<tr>
<td>TRST-</td>
<td>JTAG test reset.</td>
<td>Output</td>
<td>Input</td>
</tr>
<tr>
<td>EMU0</td>
<td>Emulation pin 0.</td>
<td>I/O</td>
<td>I/O</td>
</tr>
<tr>
<td>EMU1</td>
<td>Emulation pin 1.</td>
<td>I/O</td>
<td>I/O</td>
</tr>
<tr>
<td>PD</td>
<td>Presence detect. Indicates that the emulation cable is connected and that the target is powered up. PD should be tied to the target processor’s I/O pins Vcc.</td>
<td>Input</td>
<td>Output</td>
</tr>
<tr>
<td>TCK_RET</td>
<td>JTAG test clock return. Test clock input to the emulator. May be a buffered or unbuffered version of TCK.</td>
<td>Input</td>
<td>Output</td>
</tr>
</tbody>
</table>

Figure 3-1, 14 Pin Header Signals and Dimensions
Although you can use other headers, recommended parts include:

**straight header, unshrouded**  
DuPont Connector Systems  
part # 67996-114  

**right-angle header, unshrouded**  
DuPont Connector Systems  
part # 68405-114  

### 3.2 Bus Protocol

The IEEE 1149.1 specification covers the requirements for JTAG bus slave devices (such as the TMS320C5x family) and provides certain rules, summarized as follows:

- The TMS/TDI inputs are sampled on the rising edge of the TCK signal of the device.

- The TDO output is clocked from the falling edge of the TCK signal of the device.

When JTAG devices are daisy-chained together, the TDO of one device has approximately a half TCK cycle set up to the next device’s TDI signal. This type of timing scheme minimizes race conditions that would occur if both TDO and TDI were timed from the same TCK edge. The penalty for this timing scheme is a reduced TCK frequency.

The IEEE 1149.1 specification does not provide rules for JTAG bus master (emulator) devices.
3.3 Emulator Cable Pod Logic

Figure 3-2 shows a portion of the emulator cable pod. These are the functional features of the emulator pod:

- Signals TMS and TDI are generated from the rising edge of TCK_RET.
- Signals TMS, TDI, TCK, and TRST- are series-terminated to reduce signal reflections.
- A 10-MHz test clock source is provided. You may also provide your own test clock for greater flexibility.

![Figure 3-2, Emulator Pod Interface]
3.4 Emulator Cable Pod Signal Timing

Figure 3-3 shows the signal timings for the emulator. Table 2 defines the timing parameters for the emulator. The timing parameters are calculated from standard data sheet parts used in the emulator and cable pod. These parameters are for reference only. Spectrum Digital does not test or guarantee these timings. The emulator pod uses TCK_RET as its clock source for internal synchronization. TCK is provided as an optional target system test clock source.

![Figure 3-3, Emulator Pod Timings](image_url)

Table 2: Emulator Pod Timing Parameters

<table>
<thead>
<tr>
<th>No</th>
<th>Reference</th>
<th>Description</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>( t_{\text{TCKmin}} )</td>
<td>TCK_RET period</td>
<td>50</td>
<td>10000</td>
<td>ns</td>
</tr>
<tr>
<td>2</td>
<td>( t_{\text{TCKhighmin}} )</td>
<td>TCK_RET high pulse duration</td>
<td>15</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>3</td>
<td>( t_{\text{TCKlowmin}} )</td>
<td>TCK_RET low pulse duration</td>
<td>15</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>4</td>
<td>( t_{\text{d(XTMX)}} )</td>
<td>TMSFTDI valid from TCK_RET high</td>
<td>20</td>
<td>35</td>
<td>ns</td>
</tr>
<tr>
<td>5</td>
<td>( t_{\text{u(XTDOmin)}} )</td>
<td>TDO setup time to TCK_RET high</td>
<td>10</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>6</td>
<td>( t_{\text{h(XTDOmin)}} )</td>
<td>TDO hold time from TCK_RET high</td>
<td>4</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>
3.5 Buffering Signals Between the Emulator and the Target System

It is extremely important to provide high-quality signals between the emulator and the target device on the target system. If the distance between the emulation header and the target device is greater than 6 inches, the emulation signals must be buffered. The need for signal buffering and placement of the emulation header can be divided into two categories:

__ No signal buffering. As shown in figure 3-4, the distance between the header and the target device should be no more than 6 inches.

**Figure 3-4, No Signal Buffering**

__ Buffered emulation signals. Figure 3-5 shows the distance between the emulation header and the target device is greater than 6 inches. The target device signals--TMS, TDI, TDO, and TCK_RET are buffered through the same package.

**Figure 3-5, Buffered Emulation Signals**
The EMU0 and EMU1 signals must have pullups to Vcc. The pullup resistor value should be chosen to provide a signal rise time less than 10 uS. A 4.7k ohm resistor is suggested for most applications. EMU0-1 are I/O pins on the target device, however, they are only inputs to the emulator. In general, these pins are used in multiprocessor systems to provide global run/stop operations.

It is extremely important to provide high quality signals, especially on the processor TCK and the emulator TCK_RET signal. In some cases, this may require you to provide special PWB trace routing and to use termination resistors to match the trace impedance. The emulator pod does provide fixed series termination on the TMS, TCK, and TDI signals.

Figure 3-6 shows an application with the system test clock generated in the target system. In this application the TCK signal is left unconnected.

There are two benefits to having the target system generate the test clock:

- The emulator provides only a single 10-MHz test clock. If you generate your own test clock, you can set the frequency to match your system requirements.
- In some cases, you may have other devices in your system that require a test clock when the emulator is not connected.
Figure 3-7 shows a typical multiprocessor configuration. This is a daisy chained configuration (TDO-TDI daisy-chained), which meets the minimum requirements of the IEEE 1149.1 specification. The emulation signals in this example are buffered to isolate the processors from the emulator and provide adequate signal drive for the target system. One of the benefits of a JTAG test interface is that you can generally slow down the test clock to eliminate timing problems. Several key points to multiprocessor support are as follows:

- The processor TMS, TDI, TDO, and TCK should be buffered through the same physical package to better control timing skew.

- The input buffers for TMS, TDI, and TCK should have pullups to Vcc. This will hold these signals at a known value when the emulator is not connected. A pullup of 4.7k ohms or greater is suggested.
3.6 Emulation Timing Calculations

The following are a few examples on how to calculate the emulation timings in your system. For actual target timing parameters, see the appropriate device data sheets.

**Assumptions:**

- \( t_{su}(TTMS) \): Target TMS/TDI setup to TCK high \( 10 \text{ ns} \)
- \( t_{h}(TTMS) \): Target TMS/TDI hold from TCK high \( 5 \text{ ns} \)
- \( t_{d}(TTDO) \): Target TDO delay from TCK low \( 15 \text{ ns} \)
- \( t_{d}(bufmax) \): Target buffer delay maximum \( 10 \text{ ns} \)
- \( t_{d}(bufmin) \): Target buffer delay minimum \( 1 \text{ ns} \)
- \( t_{bufskew} \): Target buffer skew between two devices in the same package:
  \[ \frac{t_{d}(bufmax) - t_{d}(bufmin)}{2} \times 0.15 = 1.35 \text{ns} \]
- \( t_{ckfactor} \): Assume a 40/60 duty cycle clock \( 0.4 \)

**Given in Table 2:**

- \( t_{d}(XTMSmax) \): Emulator TMS/TDI delay from TCK_RET high, max \( 35 \text{ ns} \)
- \( t_{d}(XTMXmin) \): Emulator TMS/TDI delay from TCK_RET high, minimum \( 20 \text{ ns} \)
- \( t_{su}(XTDOmin) \): TDO setup time to emulator TCK_RET high \( 10 \text{ ns} \)

There are two key timing paths to consider in the emulation design:

1. the TCK_RET/TDI\(_{(tprdtck\_TMS)}\) path, and
2. the TCK_RET/TDO\(_{(tprdtck\_TDO)}\) path.

In each case, the worst case path delay is calculated to determine the maximum system test clock frequency.
Case 1: Single processor, direct connection, TMS/TDI timed from TCK RET high.

\[ t_{\text{prdtck,TMS}} = t_d(X_{\text{TMSmax}}) + t_{su}(T_{\text{TMS}}) \]
\[ = (35\text{ns} + 10\text{ns}) \]
\[ = 45\text{ns} \text{ (22.2 MHz)} \]

\[ t_{\text{prdtck,TDO}} = \frac{[t_d(T_{\text{TDO}}) + t_{su}(X_{\text{TDOmin}})]}{t_{\text{ckfactor}}} \]
\[ = (15\text{ns} + 10\text{ns}) / 0.4 \]
\[ = 62.5\text{ns} \text{ (16.0 MHz)} \]

In this case, the TCK/TDO path is the limiting factor. One other thing to consider in this case is the TMS/TDI hold time. The minimum hold time for the emulator cable pod is 20ns, which meets the 5ns hold time of the target device.

Case 2: Single/multiple processor, TMS/TDI buffered input; TCK RET/TDO buffered output, TMS/TDI timed from TCK RET high.

\[ t_{\text{prdtck,TMS}} = t_d(X_{\text{TMSmax}}) + t_{su}(T_{\text{TMS}}) + 2t_d(\text{bufmax}) \]
\[ = (35\text{ns} + 10\text{ns} + 2(10\text{ns}) \]
\[ = 65\text{ns} \text{ (15.3 MHz)} \]

\[ t_{\text{prdtck,TDO}} = \frac{(t_d(T_{\text{TDO}}) + t_{su}(X_{\text{TDOmin}}) + t_{\text{bufskew}})}{t_{\text{ckfactor}}} \]
\[ = (15\text{ns} + 10\text{ns} + 1.35\text{ns}) / 0.4 \]
\[ = 65.8\text{ns} \text{ (15.1 MHz)} \]

In this case, the TCK/TDO path is the limiting factor. The hold time on TMS/TDI is also reduced by the buffer skew (1.35 ns) but still meets the minimum device hold time.
3.7 Mechanical Dimensions of the SPI515 Adjustable Voltage JTAG Emulator

The SPI515 Adjustable Voltage Scan Path Interface Pod consists of a 3-foot 25 conductor cable, the SPI515 emulator pod, and a short section of cable that connects to the target system. The overall cable length is approximately 3 feet, 10 inches. Figure 3-8 and Figure 3-9 (page 3-12) show the mechanical dimensions for the SPI515 emulator pod and short cable. Note that the pin-to-pin spacing on the connector is 0.100 inches in both the X and Y planes. The SPI515 enclosure is nonconductive plastic with four recessed metal screws.

Note: All dimensions are in inches and are nominal dimensions, unless otherwise specified.
Note: All dimensions are in inches and are nominal dimensions, unless otherwise specified.
Chapter 4
Specifications For Your Target’s I/O Interface to the Emulator

This chapter contains information about connecting your target system’s logging interface to the SPI515 emulator. Your target system must use a special 10-pin connector for proper communication with the emulator.

<table>
<thead>
<tr>
<th>Topic</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.1 Designing Your Target System’s Logging Connector</td>
<td>4-2</td>
</tr>
<tr>
<td>4.2 Data Logging Signal Timing</td>
<td>4-3</td>
</tr>
<tr>
<td>4.3 Data Logging Circuitry</td>
<td>4-3</td>
</tr>
<tr>
<td>4.4 Data Logging Connections</td>
<td>4-4</td>
</tr>
</tbody>
</table>
4.1 Designing Your Target System’s Logging Connector (10-pin Header)

The SPI515 has a 10 pin header for bit I/O support and SPI515 data logging. When used for data logging all the bit I/O pins are used. The SOMI pin drives a constant level in version 3 and earlier of the SPI515. There is no slave-to-master channel. The DSP is the master and the SPI515 is the slave. The maximum SCLK is 20 Mhz. SIMO data should be driven by the master on the rising edge of SCLK with no delay. The SPI515 captures data on the falling edge of SCLK.

The table below shows the signals on the logging connector.

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Signal</th>
<th>Pin #</th>
<th>Signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>BitI/O-0,STE(input)</td>
<td>2</td>
<td>GND</td>
</tr>
<tr>
<td>3</td>
<td>BitI/O-1,SIMO(input)</td>
<td>4</td>
<td>GND</td>
</tr>
<tr>
<td>5</td>
<td>BitI/O-2, SCLK(input)</td>
<td>6</td>
<td>GND</td>
</tr>
<tr>
<td>7</td>
<td>BitI/O-3, SOMI(output)</td>
<td>8</td>
<td>GND</td>
</tr>
<tr>
<td>9</td>
<td>NC</td>
<td>10</td>
<td>NC</td>
</tr>
</tbody>
</table>

The figure below shows the logging connector on the emulator as viewed from the end. The position of the pins is indicated. The connector on the SPI515 is a male connector and keyed above pin 5.

Figure 4-1, 10 Pin Header Pin Positions as viewed from end of emulator

Although you can use other headers, recommended parts include:

**header, unshrouded**  AMP #: 746286-1
4.2 Data Logging Signal Timing

The signal timing for the data logging on the Bit I/O connector is shown below.

![Data Logging Signal Timing Diagram](image)

- Tclk = 50 ns. (20 Mhz.)
- tsu = 7 ns.
- th = 7 ns.
- td = 35 ns.

Figure 4-2, Data Logging Signal Timing

4.3 Data Logging Circuitry

The circuit logic for the Bit I/O 0, 1, 2, and 3 on the Bit I/O connector is shown below.

![Data Logging Circuit Logic Diagram](image)

- Input/Output levels are derived from the JTAG PD pin shown in table 1.
- Pins used for data logging cannot be used for Bit I/O.
- Output pins behave as open collector. For faster rise time on output turn off, the user may include a pullup resistor with connection to the same power supply that sources the JTAG PD pin. The minimum external pullup is 100 ohms.
4.4 Data Logging Connections

Figure 4-4 below shows the suggested DSP connection.

![Figure 4-4, Suggested DSP Connection](image)

Figure 4-5 below shows an alternate DSP connection.

![Figure 4-5, Alternate DSP Connection](image)

* If future support is required:
  
  $R = 1\, \text{K ohm typical}$
  
  $R$ may be lowered to increase SCLK frequency.
  
  Output pins behave as open collector. For faster rise time on output turn off, the user may include a pullup resistor with connection to the same power supply that sources the JTAG PD pin. The minimum value of $R$, the external pullup is 100 ohms with DSP Vcc = 3.6 volts.