SPECTRUM DIGITAL INCORPORATED

SPI525 PCI BUS Scan Path Emulator

Installation Guide

2000 DSP Development Systems

SPI525 PCI Bus
Scan Path Emulator
Installation Guide

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PATENTS

A patent application has been filed regarding the technology used in the SPI525 PCI Bus Scan Path Emulator.

Contents

Chapter 1

Introduction to the Adjustable Voltage Pod

This chapter provides a description of the Adjustable Voltage Pod and it's key features.

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1.0 Overview of the Adjustable Voltage Emulator Pod

The modular JTAG emulator pod is designed to be used with digital signal processors and microprocessors which operate between +0.8 volts to +5 volts. Since this emulator is powered from the PCI adapter card, no external power connection is necessary.

The target JTAG operating voltage levels can be manually selected via a 16-position switch. Feedback on the selected levels is indicated by status LEDs. The voltage selector switch and status LEDs are present on the adjustable voltage emulator pod for convenient use.

The adjustable voltage emulator pod is designed to work with Spectrum Digital's SPI525 PCI Bus emulation adapter card.

1.1 Key Features of the Adjustable Voltage Emulator Pod

The adjustable voltage emulator pod has the following features:

- Supports Texas Instrument's Digital Signal Processors and Microcontrollers with JTAG interface (IEEE 1149.1)
- Compatible with Spectrum Digital's SPI525 PCI Bus emulation adapter card.
- Compatible with Spectrum Digital's SPI510 ISA Bus emulation adapter card.
- Adjustable input and output voltage levels for low voltage devices.
- Four status LEDs for self-test and voltage levels.
- Incorporates EMU0/EMU1 hold reset features for TMS27xx DSPs.
- Power provided by PCI adapter card.
- Compatible with Code Composer Integrated Development Environment

1.2 Key Items on the Adjustable Voltage Pod

Figure 1-1 shows the adjustable voltage pod and SPI525 PCI Bus Adapter card. The key items identified are:

- Status LEDs
- JTAG connector
- Tail
- Voltage selection switch
- DB-25 connector to the host adapter card
- SPI525 PCI Adapter Card

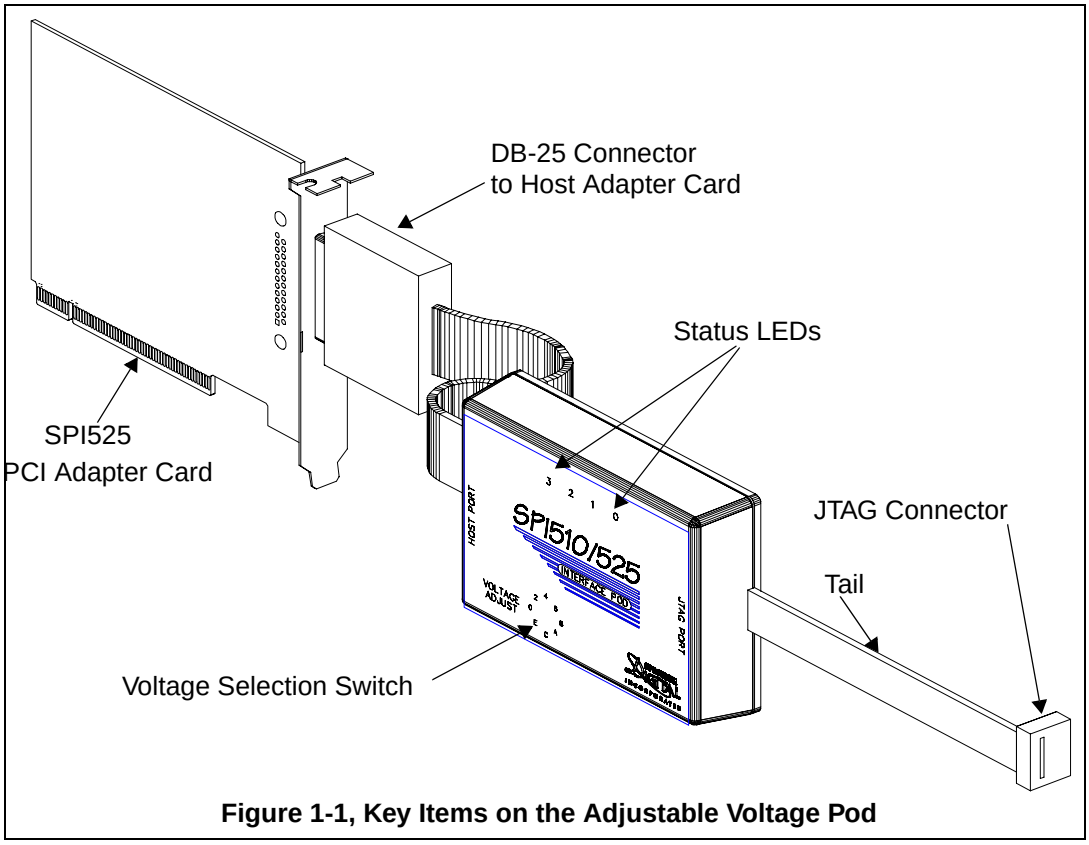

Figure 1-1, Key Items on the Adjustable Voltage Pod

Chapter 2

Installing the SPI525 PCI Bus Adapter Card

This chapter contains installation instructions for the SPI525 PCI bus adapter card for use with the adjustable voltage emulator pod.

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2.1 What You'll Need

To install the SPI525 PCI bus adapter card the following hardware will be needed:

__	**host**	An IBM PC/AT or 100% compatible PCI/EISA-based PC
__	**slot**	One PCI slot
__	**emulator adapter card**	Spectrum Digital SPI525 PCI bus adapter card
__	**JTAG cable**	Adjustable Voltage Emulator Pod
__	**target system**	A board with a JTAG based TI DSP or Microcontroller and power supply
__	**connector to target system**	14-pin connector (two rows of seven pins) --- see Chapter 4 for more information about this connector

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WARNING !

Minimizing Static Shock

Special handling methods and material should be used to prevent equipment damage. You should be familiar with identification and handling of ESD sensitive devices before attempting to perform procedures described in this manual.

2.2 Placing the SPI525 PCI Adapter Into Your PC

Follow the steps below to place the SPI525 PCI Adapter card into your PC.

WARNING

Minimizing Personal Injury:

To minimize the risk of personal injury, ***always*** turn off the power to your PC and unplug the power cord before installing the SPI525 PCI adapter.

- ❑ Turn the power to your PC off and unplug the power cord
- ❑ Remove the cover of your PC.
- ❑ Remove the mounting bracket from an unused PCI slot.
- ❑ Carefully but firmly push the SPI525 PCI bus adapter into a PCI slot.
- ❑ Return the mounting screw to the mounting bracket on the SPI525 PCI bus adapter and tighten the screw.
- ❑ Replace the cover on the PC.

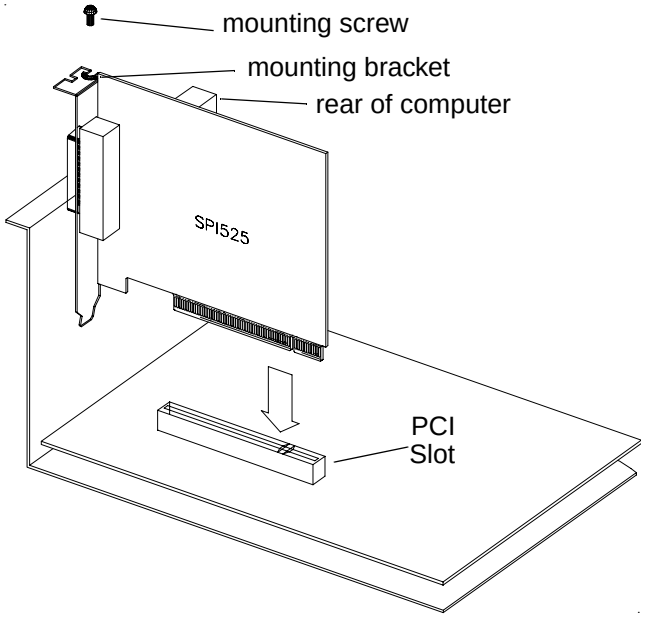

Figure 1-1, Placing the SPI525 Into Your PC

2.3 What to do next

Now that your SPI525 PCI Adapter is installed, continue to Chapter 3 for adjustable voltage pod installation instructions.

Chapter 3

Installing the Adjustable Voltage Pod

This chapter contains installation instructions for the adjustable voltage pod used with Spectrum Digital SPI525 PCI bus adapter card. For use with specific software packages such as debuggers or TI's Code Composer refer to their respective documentation.

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NOTE

When using the adjustable voltage pod, install the PCI adapter first per the instructions in chapter 2 of this document.

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3.1 What You'll Need

The following checklists detail items shipped with the adjustable voltage emulator pod and additional items needed to use these tools.

Hardware checklist

__	**host**	An IBM PC/AT or 100% compatible PCI/EISA-based PC
__	**emulator adapter**	Spectrum Digital SPI525 PCI Adapter card
__	**emulator module**	Adjustable Voltage Scan Path Emulator Pod
__	**target system**	A board with a JTAG based TI DSP or Microcontroller and power supply
__	**connector to target system**	14-pin connector (two rows of seven pins) --- see Chapter 4 for more information about this connector

Software checklist

__	**operating system**	Win 95, Win 98, or Win NT 4.0
__	**software tools**	Compiler/assembler/linker for DSP or Microcontroller
__	**debugger**	TI Code Composer Debug Tools, and TI Code Composer.
__	**drivers** [t]	drivers for TI Code Composer

[t] Included as part of the SPI525 package

3.2 Voltage Selection Switch

The adjustable voltage pod has a 16-position voltage selection switch that must be correctly set before using the emulator. This switch is accessible through the front of the emulator and is present just to the left of the Spectrum Digital logo. Table 1 below shows the 16-switch positions and their respective input and output voltage levels, and target system voltages.

The Signal Output Voltage is the voltage level on the TMS, TDI, TCK, and TRST pins.

The Signal Input Threshold is the voltage level on the TCK_RET, TDO, EMU0, and EMU1 pins.

WARNING !

The Power Detect Input Threshold is the voltage level on the PD pin. This switch should be set prior to applying power to the DSP target board.

Table 1: Voltage Selection Switch

Rotary Switch Position	Signal Output Voltage	Signal Input Threshold	Power Detect Input Threshold	Target System Voltage
0	0.000	0.000	0.661	Reserved
1	0.000	0.000	0.661	Reserved
2	0.000	0.000	0.661	Reserved
3	0.000	0.000	0.661	Reserved
4	1.000	0.600	0.661	0.09 - 1.1
5	1.200	0.720	0.793	1.1 - 1.3
6	1.400	0.840	0.925	1.3 - 1.5
7	1.600	0.960	1.057	1.5 - 1.7
8	1.800	1.080	1.190	1.7 - 1.9
9	2.000	1.200	1.322	1.9 - 2.1
A	2.200	1.320	1.454	2.1 - 2.3
B	2.400	1.440	1.586	2.3 - 2.5
C	2.600	1.560	1.719	2.5 - 2.7
D	2.800	1.680	1.851	2.7 - 2.9
E	3.000	1.800	1.983	2.9 - 3.2
*F	3.200	1.920	2.115	3.2 - 5.0

*Default Setting
Note: Positions 0-3 are reserved

3.3 Installing the Adjustable Voltage Pod

This section contains the steps for installing the adjustable voltage pod.

WARNING

Target Cable Connectors:

Be very careful with the target cable connectors. connect them gently; don't force them into position, or you may damage the connectors.

Do **not** connect or disconnect the DB-25 connector while the PC is powered up.

Do **not** connect or disconnect the 14-pin cable while the target system is powered up.

3.3.1 Adjustable Voltage Pod Installation Checklist

To install the adjustable voltage pod, execute the following checklist:

❑ Turn off the power to your PC and install the Spectrum Digital SPI525 PCI Bus Emulator Adapter card

❑ Turn off the power to your target system

❑ Attach the adjustable voltage pod DB-25 connector to the PCI Bus Emulator Adapter card in the PC.

❑ Turn on the power to your PC and allow it to boot up. The adjustable voltage pod will go through the "Power Detection Sequence" detailed in section 3.5

❑ Set the 16-position switch on the adjustable voltage pod to reflect the target input voltage on the PD pin of the 14-pin connector, or your desired voltage. This voltage is shown in column 4 of table 1, shown in section 3.2.

Note:

Some target systems put 5 volts on the PD pin for 3-volt systems.

❑ Plug the tail of the adjustable voltage pod (14 pin ribbon cable) on to the 14-pin header on the SPI525 PCI Emulator card.

❑ Your system configuration should now look like that in Figure 3.1 on the following page.

❑ Apply power to your target.

Figure 3-1 shows how you connect the SPI525 in a typical system configuration with a host PC and target board.

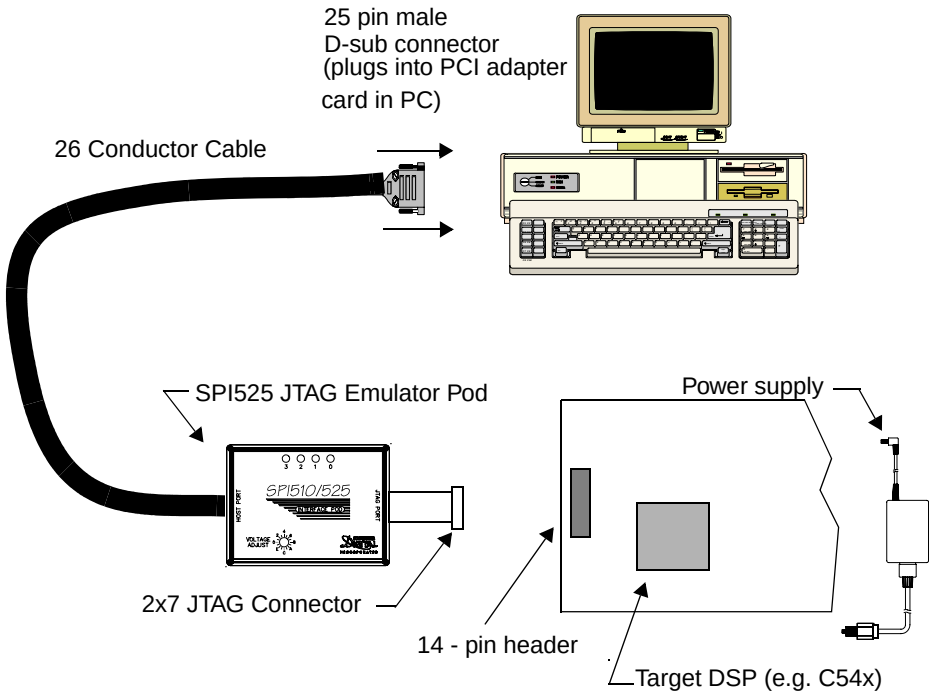

Figure 3-1, Connecting the SPI525 To Your Target System

3.4 Adjustable Voltage Emulator Pod LEDs

The adjustable voltage emulator pod has 4 red Light Emitting Diodes (LEDs). These LEDs provide the user with the status of the emulator. An LED “On” indicates a 1 value, and LED “off” indicates a 0 value. The meaning of each LED is described below.

LED 0: Flashes when the target power falls below the Power Detect Input Threshold voltage.

LED 1: Flashes when the target power has been detected but the SPI525 PCI adapter card has NOT reset the TRST signal.

LED 3: On when EMU0 is in the “Hold-In-Reset” state. LED 0 or LED 1 should also be flashing at this time.

LED 0-3: The steady state “On” values reflects the switch position in hexadecimal format with LED 0 being the LSB.

3.5 Adjustable Voltage Emulator Pod Power Detection Sequence

The procedure below describes the sequence that the adjustable voltage emulator pod goes though to detect power on the PD pin of the 14 pin JTAG header:

1. When the cable is plugged into the SPI525 PCI adapter card and power is applied to the adjustable voltage emulator pod, LEDs 0-3 will scroll for approximately 6 seconds.

2. The 16-position rotary switch is read and the voltages are set per the table 1 in section 2.2.

3. The PD (Presence Detect) pin on the 14 pin header is monitored until it’s voltage level exceeds the Power Detect Input Threshold. LED 0 will flash until this condition is met.

4. When the target power is detected the JTAG outputs of the SPI525 will be enabled.

5. Once the JTAG outputs are enabled the TRST line is monitored and LED 1 will flash until TRST is taken high by the emulator software driver. Once TRST is taken high EMU0 will be released from it’s “Wait-In-Reset” value and return to a tri-state condition. LED 3 will then turn off.

6. When target power is detected and TRST is high the LEDs 0-3 will reflect the rotary switch setting.

7. The PD and TRST pins are monitored continuously. If either signal drops below it’s high threshold then the power detection sequence will start over at step #2.

Notes:

1. It is recommended that you set your rotary switch settings while the target processor is powered off and the LED 0 is flashing

2. If you change the rotary switch setting after the SPI525 has reached it's steady state (step # 6) the new switch setting is ignored until either the PD or TRST signal levels drop below their logic high threshold.

3. The TRST pin is toggled by the software reset utility (e.g. *emurst.exe*) and by low level emulation software drivers. If LED 1 is flashing then execute *emurst.exe* and check to see if the LEDs go to a steady state and that the hexadecimal value on the LEDs match your rotary switch setting.

3.5.1 WAIT-IN-RESET

Newer TI DSPs (e.g. TMS320C27x) have a feature called Wait-In-Reset. When the SPI525 detects the loss of target poser, it will drive EMU0 to 0 volts. When the target system is powered on and EMU0 = 0 volts, EMU1 = Vcc, and TRSTn = 0 volts then the DSP will hold in reset until the debugger is started. On processors that do not support Wait-In-Reset" pulling EMU0 should have no effect. EMU0 is tri-stated within 20 milliseconds after TRST returns high. A 100 ohm resistor is included in the event that the target system is driving this signal. Normally this signal is pulled high on the target system with a 4.7K ohm or larger resistor.

Chapter 4

Specifications For Your Target System's Connection to the Emulator

This chapter contains information on connecting the target system to the emulator. The target system must use a special 14-pin connector for proper communication with the emulator.

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4.1 Designing Your Target System's Emulator Connector (14-pin Header)

Certain devices support emulation through a dedicated emulation port. This port is a superset of the IEEE 1149.1 (JTAG) standard and is accessed by the emulator. To perform emulation with the emulator, your target system must have a 14-pin header 2 rows of 7 pins) with the connections that are shown in Figure 4-1. Table 1 describes the emulation signals.

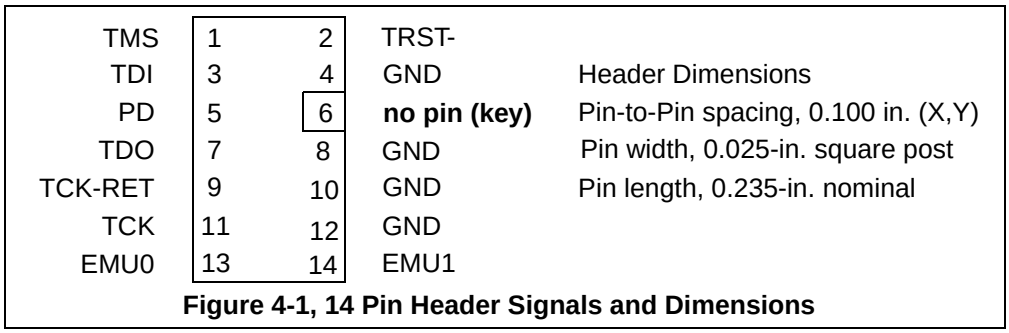

Figure 4-1, 14 Pin Header Signals and Dimensions

Table 1: 14-Pin Header Signal Description

Signal	Description	Emulator State	Target State
TMS	JTAG test mode select.	Output	Input
TDI	JTAG test data input.	Output	Input
TDO	JTAG test data output.	Input	Output
TCK	JTAG test clock. TCK is a 10-MHz clock source from the emulation pod. This signal can be used to drive the system test clock.	Output	Input
TRST-	JTAG test reset.	Output	Input
EMUO	Emulation pin 0.	I/O	I/O
EMU1	Emulation pin 1.	Input	I/O
PD	Presence detect. Indicates that the emulation cable is connected and that the target is powered up. PD should be tied to the target processor's I/O pins Vcc.	Input	Output
TCK_RET	JTAG test clock return. Test clock input to the emulator. May be a buffered or unbuffered version of TCK.	Input	Output

Although you can use other headers, recommended parts include:

straight header, unshrouded	DuPont Connector Systems part # 67996-114
right-angle header, unshrouded	DuPont Connector Systems part # 68405-114

4.2 Bus Protocol

The IEEE 1149.1 specification covers the requirements for JTAG bus slave devices (such as the TMS320C5x family) and provides certain rules, summarized as follows:

__ The TMS/TDI inputs are sampled on the rising edge of the TCK signal of the device.

__ The TDO output is clocked from the falling edge of the TCK signal of the device

When JTAG devices are daisy-chained together, the TDO of one device has approximately a half-TCK cycle set up to the next device's TDI signal. This type of timing scheme minimizes race conditions that would occur if both TDO and TDI were timed from the same TCK edge. The penalty for this timing scheme is a reduced TCK frequency.

The IEEE 1149.1 specification does not provide rules for JTAG bus master (emulator) devices.

4.3 Emulator Cable Pod Logic

Figure 4-2 shows a portion of the emulator cable pod. These are the functional features of the emulator pod:

- Signals TMS and TDI are generated from the rising edge of TCK_RET.
- Signals TMS, TDI, TCK, and TRST- are series-terminated to reduce signal reflections.
- A 10-MHz test clock source is provided. You may also provide your own test clock for greater flexibility.

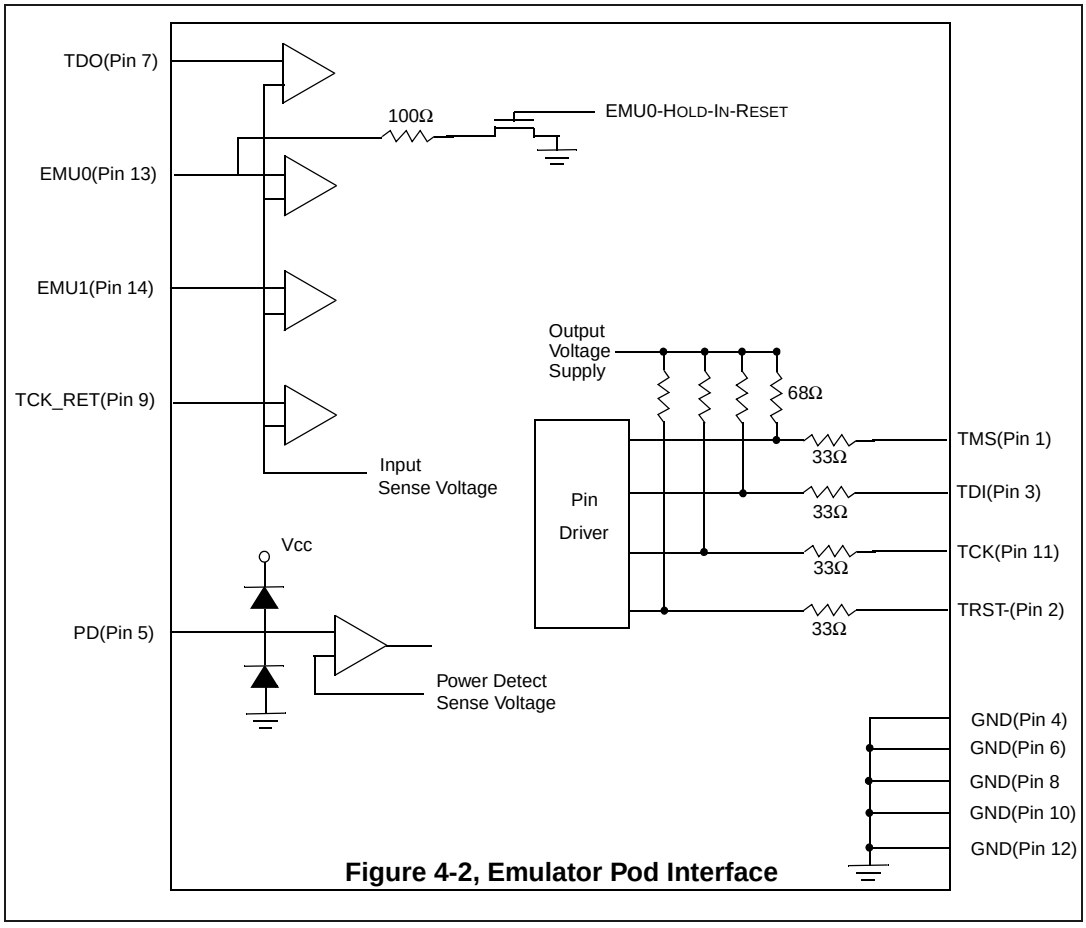

Figure 4-2, Emulator Pod Interface

4.4 Emulator Cable Pod Signal Timing

Figure 4-3 shows the signal timings for the emulator. Table 2 defines the timing parameters for the emulator. The timing parameters are calculated from standard data sheet parts used in the emulator and cable pod. These parameters are for reference only. Spectrum Digital does not test, nor does it guarantee these timings. The emulator pod uses TCK_RET as its clock source for internal synchronization. TCK is provided as an optional target system test clock source.

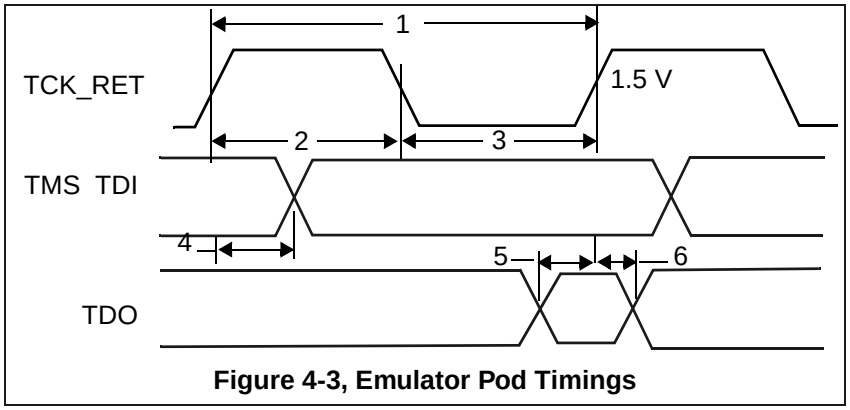

Figure 4-3, Emulator Pod Timings

Table 2: Emulator Pod Timing Parameters

No	Reference	Description	Min	Max	Units
1	t_{TCKmin}	TCK_RET period	50	200	ns
2	$t_{TCKhighmin}$	TCK_RET high pulse duration	15		ns
3	$t_{TCKlowmin}$	TCK_RET low pulse duration	15		ns
4	$td_{(XTMX)}$	TMSFTDI valid from TCK_RET high	20	44	ns
5	$tsu_{(XTDOmin)}$	TDO setup time to TCK_RET high	3		ns
6	$thd_{(XTDOmin)}$	TDO hold time from TCK_RET high	12		ns

4.5 Buffering Signals Between the Emulator and the Target System

It is extremely important to provide high-quality signals between the emulator and the target device on the target system. If the distance between the emulation header and the target device is greater than 6 inches, the emulation signals must be buffered. The need for signal buffering and placement of the emulation header can be divided into two categories:

— **No signal buffering.** As shown in figure 4-4, the distance between the header and the target device should be no more than 6 inches.

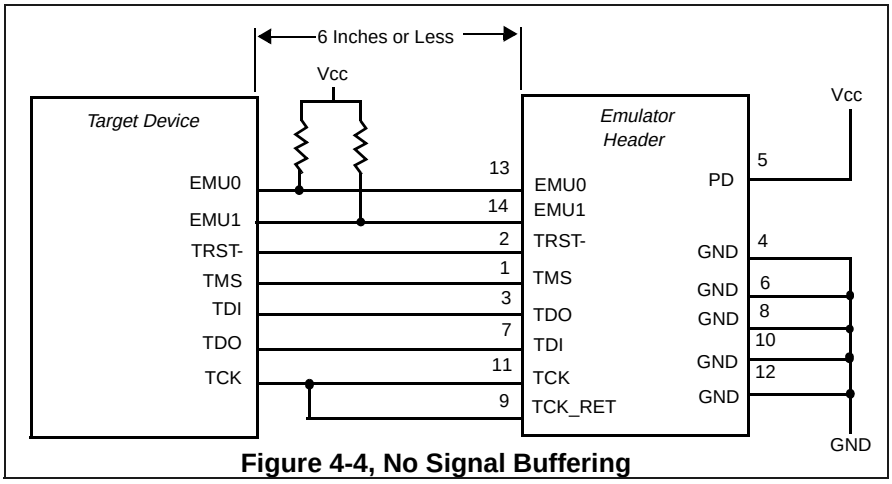

Figure 4-4, No Signal Buffering

— **Buffered emulation signals.** Figure 4-5 shows the distance between the emulation header and the target device is greater than 6 inches. The target device signals--TMS, TDI, TDO, and TCK_RET are buffered through the same package.

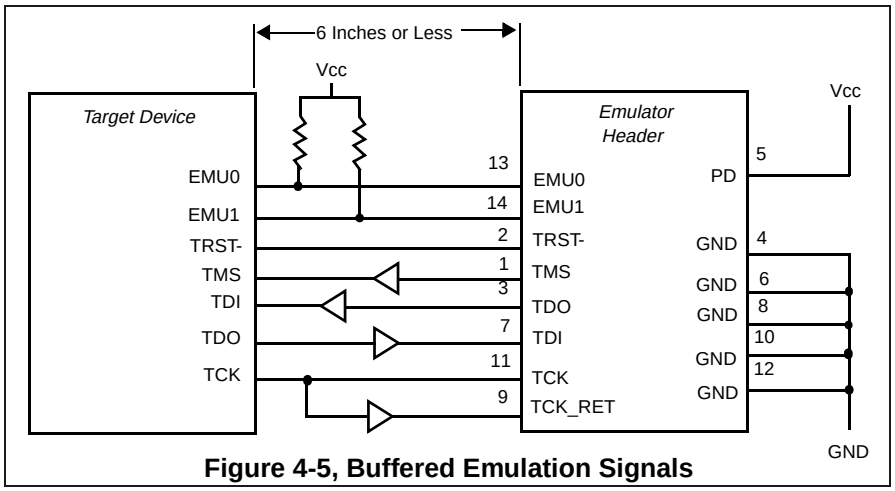

Figure 4-5, Buffered Emulation Signals

- The EMU0 and EMU1 signals must have pull-ups to Vcc. The pull-up resistor value should be chosen to provide a signal rise-time less than 10 uS. A 4.7K ohm resistor is suggested for most applications. EMUO-1 are I/O pins on the target device. However, they are only inputs to the emulator. In general, these pins are used in multiprocessor systems to provide global run/stop operations.

- It is extremely important to provide high quality signals, especially on the processor TCK and the emulator TCK_RET signal. In some cases, this may require you to provide special PWB trace routing and to use termination resistors to match the trace impedance. The emulator pod does provide fixed series termination on the TMS, TCK, and TDI signals.

Figure 4-6 shows an application with the system test clock generated in the target system. In this application the TCK signal is left unconnected.

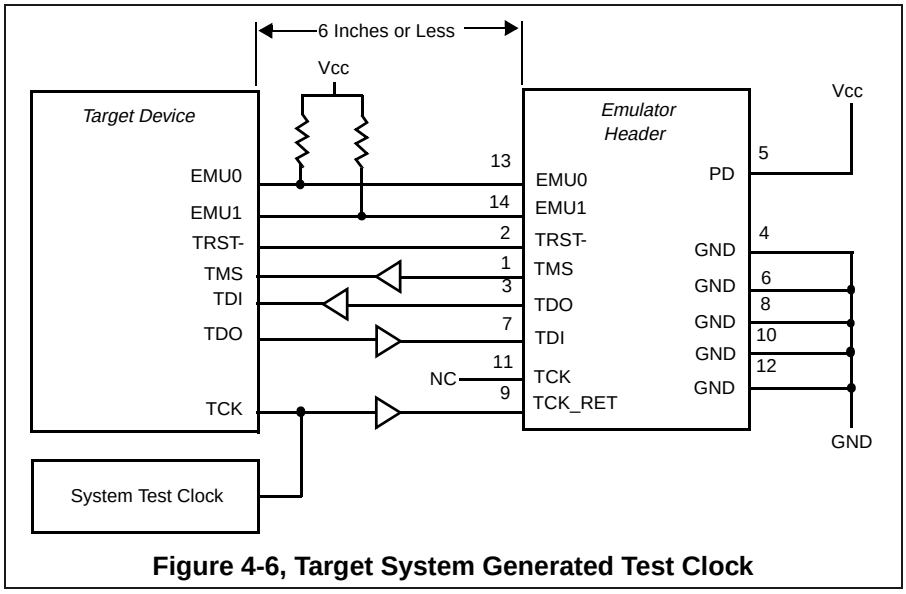

Figure 4-6, Target System Generated Test Clock

There are two benefits to having the target system generate the test clock:

- The emulator provides only a single 10-MHz test clock. If you generate your own test clock, you can set the frequency to match your system requirements.

- In some cases, you may have other devices in your system that require a test clock when the emulator is not connected.

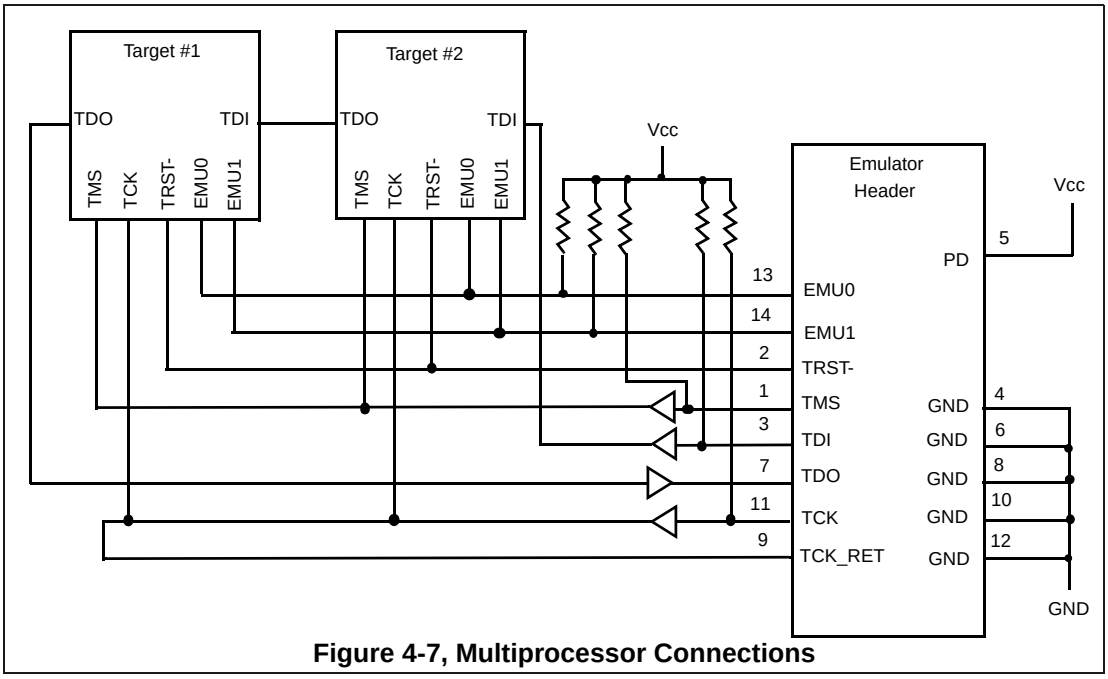

Figure 4-7, Multiprocessor Connections

Figure 4-7 shows a typical multiprocessor configuration. This is a daisy-chained configuration (TDO-TDI daisy-chained), which meets the minimum requirements of the IEEE 1149.1 specification. The emulation signals in this example are buffered to isolate the processors from the emulator and provide adequate signal drive for the target system. One of the benefits of a JTAG test interface is that you can generally slow down the test clock to eliminate timing problems. Several key points to multi-processor support are as follows:

- The processor TMS, TDI, TDO, and TCK should be buffered through the same physical package to better control timing skew.
- The input buffers for TMS, TDI, and TCK should have pull-ups to Vcc. This will hold these signals at a known value when the emulator is not connected. A pull-up of 4.7K ohms or greater is suggested.

4.6 Emulation Timing Calculations

The following are a few examples calculating the system emulation timings system. For actual target timing parameters, see the appropriate device data sheets.

Assumptions:

$t_{su(TTMS)}$	Target TMS/TDI setup to TCK high	10	ns
$t_{h(TTMS)}$	Target TMS/TDI hold from TCK high	5	ns
$t_{d(TTDO)}$	Target TDO delay from TCK low	15	ns
$t_{d(bufmax)}$	Target buffer delay maximum	10	ns
$t_{d(bufmin)}$	Target buffer delay minimum	1	ns
$t_{(bufskew)}$	Target buffer skew between two devices in the same package: $[t_{d(bufmax)} - t_{d(bufmin)}] \times 0.15$	1.35	ns
$t_{tckfactor}$	Assume a 40/60 duty cycle clock		0.4

Given in Table 2:

$t_{d(XTMX)}$	min emulator TMS/TDI delay from TCK_RET low, minimum	6	ns
$t_{d(XTMSmax)}$	Emulator TMS/TDI delay from TCK_RET high, max	44	ns
$t_{d(XTMXmin)}$	Emulator TMS/TDI delay from TCK_RET high, minimum	20	ns
$t_{su(XTDOmin)}$	TDO setup time to emulator TCK_RET high	3	ns

There are two key timing paths to consider in the emulation design:

__ the TCK_RET/TDI(t_{prdtck_TMS}) path, and
__ the TCK_RET/TDO(t_{prdtck_TDO}) path.

In each case, the worst case path delay is calculated to determine the maximum system test clock frequency.

Case 1: Single processor, direct connection, TMS/TDI timed from TCK_RET high.

t_{prdtck_TMS} = $t_{d(XTMSmax)} + t_{su(TTMS)}$
= (44ns + 10ns)
= 54ns (18.5 MHz)

t_{prdtck_TDO} = $[t_{d(TTDO)} + t_{su(XTDOmin)}] / t_{tckfactor}$
= (15ns + 3ns) / 0.4
= 45ns (22.2 MHz)

In this case, the TCK/TDO path is the limiting factor. One other thing to consider in this case is the TMS/TDI hold time. The minimum hold time for the emulator cable pod is 20ns, which meets the 5ns hold time of the target device.

Case 2: Single/multiple processor, TMS/TDI buffered input; TCK_RET/TDO buffered output, TMS/TDI timed from TCK_RET high.

t_{prdtck_TMS} = $t_{d(XTMSmax)} + t_{su(TTMS)} + 2t_{d(bufmax)}$
= (44ns + 10ns + 2(10ns)
= 74ns (13.5 MHz)

t_{prdtck_TDO} = $(t_{d(TTDO)} + t_{su(XTDOmin)} + t_{bufskew}) / t_{tckfactor}$
= (15ns + 3ns + 1.35 ns) / 0.4
= 58.4ns (20.7 MHz)

In this case, the TCK/TMS path is the limiting factor. The hold time on TMS/TD is also reduced by the buffer skew (1.35 ns) but still meets the minimum device hold time.

Appendix A

Adjustable Voltage Pod Mechanicals

This appendix contains the mechanicals for the SPI525 DSK. The schematics were drawn on ORCAD.

A.1 Mechanical Dimensions of the Adjustable Voltage Pod

The adjustable voltage pod consists of a 3-foot, 25-conductor cable, emulator pod, and a short section of cable that connects to the target system. The overall cable length is approximately 3 feet, 10 inches.
Figure 4-8 and Figure 4-9 (page 4-12) show the mechanical dimensions for the adjustable voltage pod and short cable. Note that the pin-to-pin spacing on the connector is 0.100 inches in both the X and Y planes. The adjustable voltage pod enclosure is nonconductive plastic with four recessed metal screws.

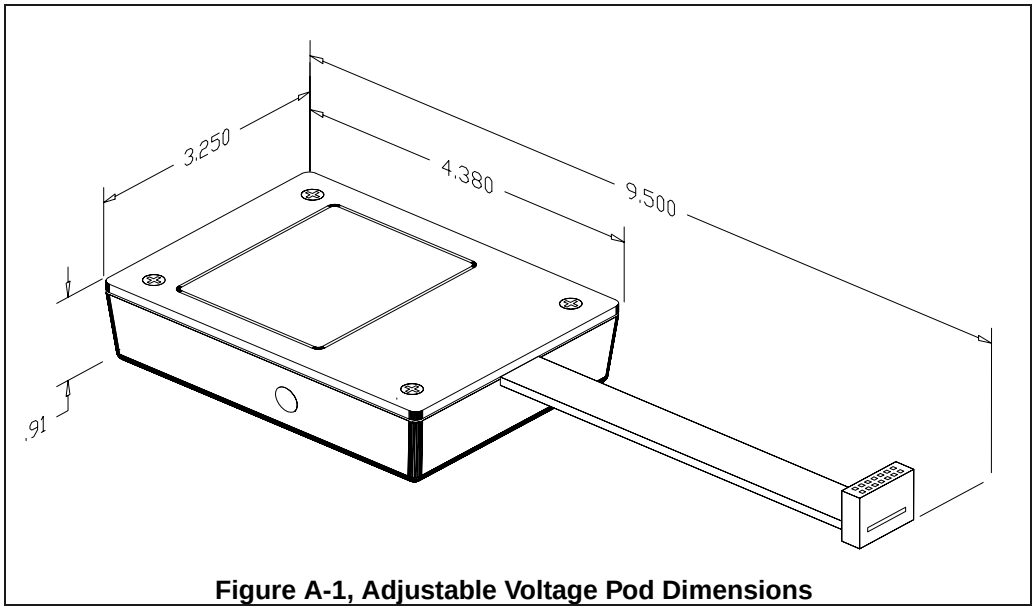

Figure A-1, Adjustable Voltage Pod Dimensions

Note: All dimensions are in inches and are nominal dimensions, unless otherwise specified.

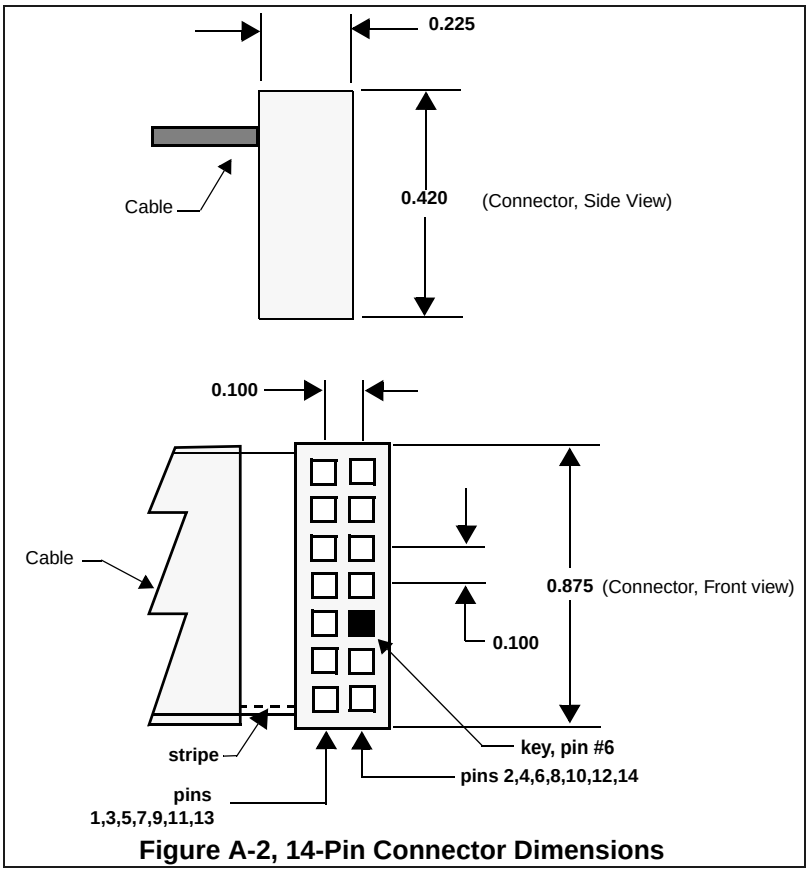

Figure A-2, 14-Pin Connector Dimensions

Note: All dimensions are in inches and are nominal dimensions, unless otherwise specified

[redacted]

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