

XDS510 USB Galvanic JTAG Emulator

*Technical
Reference*

***XDS510 USB Galvanic
JTAG Emulator
Installation Guide***

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About This Manual

This document describes the module level operations of the XDS510 USB Galvanic JTAG Emulator. This emulator is designed to be used with digital signal processors (DSPs) and microcontrollers designed by Texas Instruments.

The XDS510 USB Galvanic JTAG Emulator is a table top module that attaches to a personal computer or laptop to allow hardware engineers and software programmers to develop applications with DSPs and microcontrollers.

Notational Conventions

This document uses the following conventions.

The XDS510 USB Galvanic JTAG Emulator will sometimes be referred to as the XDS510 USB Galvanic, JTAG Emulator, or Emulator.

Program listings, program examples, and interactive displays are shown in a special italic typeface. Here is a sample program listing.

```
equations  
!rd = !strobe&rw;
```

Information About Cautions

This book may contain cautions.

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software, or hardware, or other equipment. The information in a caution is provided for your protection. Please read each caution carefully.

Related Documents

Texas Instruments Code Composer and Code Composer Studio Users Guide

Chapter 1

Introduction to the XDS510 USB Galvanic JTAG Emulator

This chapter provides you with a description of the XDS510 USB Galvanic JTAG Emulator along with the key features.

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1.0 Overview of the XDS510 USB Galvanic JTAG Emulator

The XDS510 USB Galvanic JTAG Emulator is designed to be used with digital signal processors (DSPs) and microprocessors which operate with +3.3 or +5 volt levels on the JTAG interface. This emulator is powered from USB line and the target system. This means no power is drawn from the target system.

The XDS510 USB Galvanic JTAG Emulator is compatible with the existing Spectrum Digital XDS510 USB JTAG emulator and operate with debuggers provided by Texas Instruments.

1.1 Key Features of the XDS510 USB Galvanic JTAG Emulator

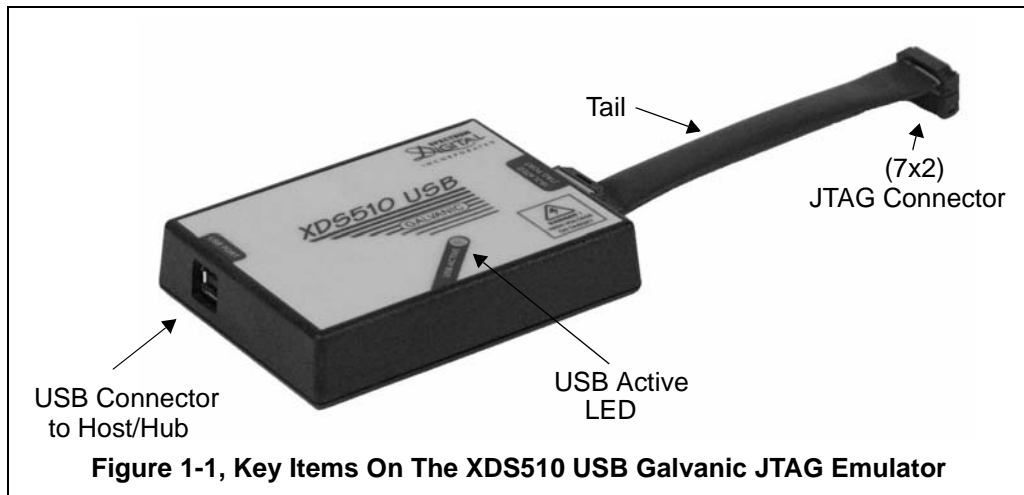
The XDS510 USB Galvanic JTAG Emulator has the following features:

- Supports Texas Instrument's Digital Signal Processors (C2xxx, C54xx, C55xx, C67xx, C64xx, TMS470, OMAP) with JTAG interface (IEEE 1149.1)
- Compatible with Spectrum Digital's XDS510 USB JTAG emulator.
- Voltage isolation provided by IL715, IL717, HCPL-260L (UL1577 rated for 2500Vrms for 1 minute and IEC 61010-1, Pollution Degree II, Material Group III, Max Working Voltage 300 Vrms Common Mode Transient Immunity 30Kv/us @ Vcm=300V)
- Voltage isolation on PWB with 6mm. minimum clearances and creepage distances
- Compatible with USB 1.x and USB 2.0 (full speed)
- Supports USB interface with host PC, no adapter card required.
- Supports +3.3 volt and +5 volt JTAG interfaces (+3.3V to +1.8V with Low Voltage Adapter).
- One status LED for USB operational status.
- Power provided by host USB port or USB hub and target system
- Compatible with Texas Instruments Code Composer Studio
- Works with emulation driver releases 2.21.03 or higher
- Compatible with Spectrum Digital's Flash programming utility
- Compatible with Windows 2000, and Windows XP Operating Systems

1.2 Key Items on the XDS510 USB Galvanic JTAG Emulator

Figure 1-1 shows the XDS510 USB Galvanic JTAG Emulator. The key items identified are:

- Status LEDs
- JTAG connector
- Tail
- USB connector to the host PC or hub



1.3 Industry Specific Support

The XDS510 USB Galvanic JTAG emulator was designed to provide limited voltage isolation in developing applications dealing with motor, power supplies, industrial control, and automated test equipment.

WARNING !

This unit may not be suited for all high voltage development or test environments

Chapter 2

Installing the XDS510 USB Galvanic JTAG Emulator

This chapter helps you install the XDS510 USB Galvanic JTAG Emulator. For use with specific software packages such as the TI's Code Composer Studio refer to their respective documentation.

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2.1 What You'll Need

The following checklists detail items that are shipped with the XDS510 USB Galvanic JTAG emulator and additional items you'll need to use these tools.

Hardware checklist

- ___ **host** An IBM PC/AT or 100% compatible PC or laptop (2 Ghz. or faster) with a hard-disk system, CD-ROM disk drive, and a free USB port
- ___ **memory** Minimum of 500MB of RAM
- ___ **display** Color SVGA or LCD
- ___ **emulator module** XDS510 USB Galvanic JTAG emulator
- ___ **target system** A board with a TI DSP or Microcontroller and power supply
- ___ **connector to target system** 14-pin connector (two rows of seven pins) --- see Chapter 3 for more information about this connector

Software checklist

- ___ **operating system** Windows 2000 SP4, Windows XP Pro SP1&2, Win XP Home SP 1&2
- ___ **software tools** Compiler/assembler/linker for DSP or Microcontroller
- ___ **debugger** Code Composer or Code Composer Studio
- ___ **drivers** Spectrum Digital drivers for TI Code Composer (included with XDS510 USB Galvanic emulator or available from Spectrum Digital's support website: <http://support.spectrumdigital.com/>)

2.2 Installing the XDS510 USB Galvanic JTAG Emulator

This section contains the steps for installing the XDS510 USB Galvanic JTAG Emulator.

WARNING

Target Cable Connectors:

Be very careful with the target cable connectors. connect them gently; don't force them into position, or you may damage the connectors.

Do **not** connect or disconnect the 14-pin cable while the target system is powered up.

2.2.1 XDS510 USB Galvanic JTAG Emulator Installation Checklist

To install the XDS510 USB Galvanic JTAG emulator drivers execute the following checklist:

- Insert the installation CD into the CD-ROM Drive. An install screen should appear, if not, go to Windows Explorer and run launch.exe from the CD ROM.

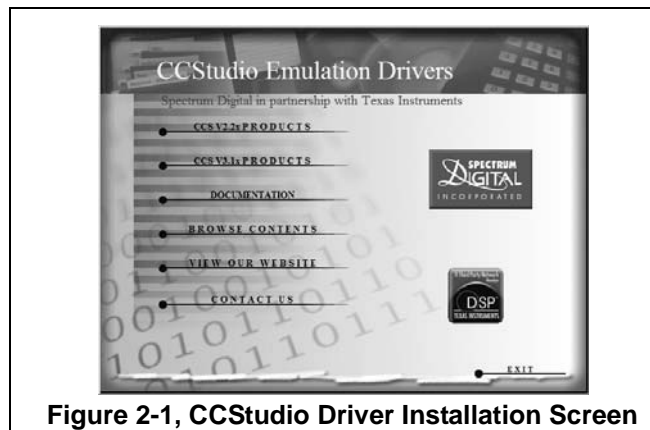
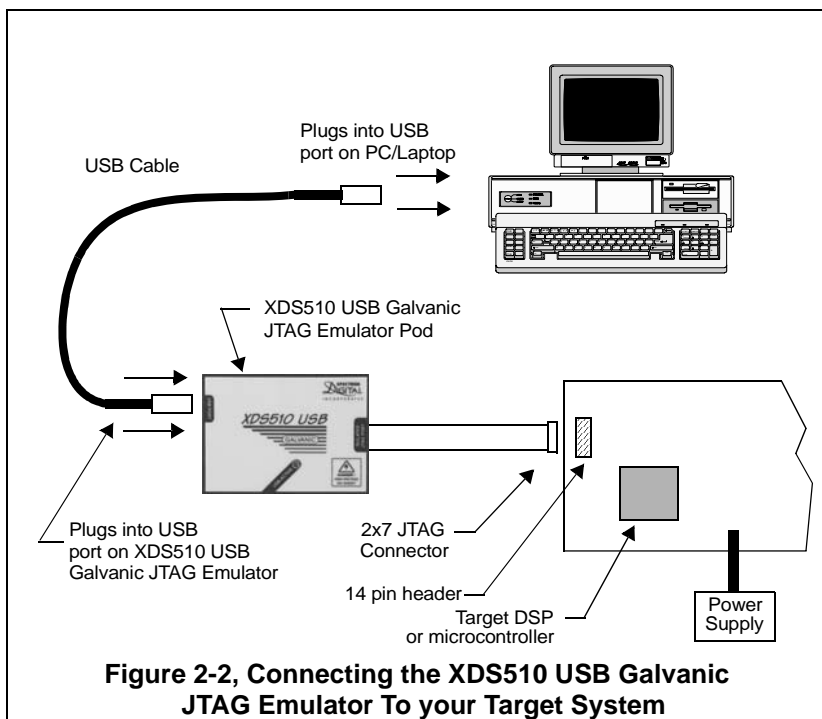


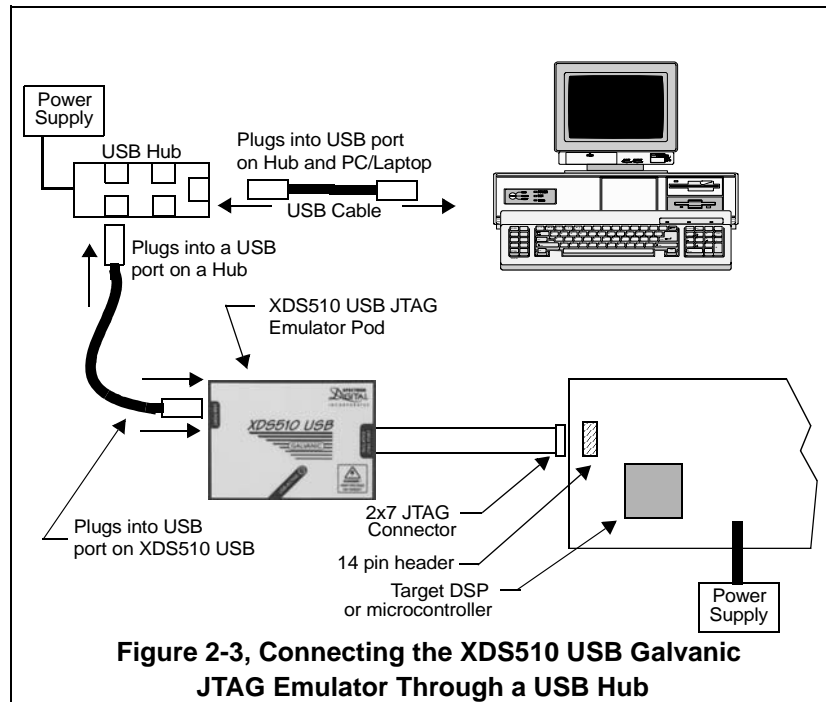
Figure 2-1, CCStudio Driver Installation Screen

- Select the CCStudio product version and then the processor on interest. For CCS 2.2x drivers you have the choice of C2000, C6000 and OMAP(C54/C55/ARM). For CCS 3.1 Platinum there is only one choice and it includes all processors in one install. When installing emulation drivers the default install should be changed to the same directory as you targeted CCStudio install. for CCS 2.2x this is normally "c:\ti" and for CCS 3.1x this is normally "C:\CCStudio_v3.1".
- Plug the supplied USB cable into an available port on your PC or HUB. Use of a USB HUB is recommended as it provides added isolation between your debug environment and PC.

- ❑ Plug the XDS510 USB Galvanic JTAG Emulator into the other end of the supplied USB cable. Windows will recognize a new USB device and pop-up the new hardware found wizard. Follow the instructions and let Windows find the USB drivers located on the install CD (sdusbem.sys and sd510u2.inf). If properly installed Windows will create a new device class named “SD USB Based Debug Tools”. The XDS510-USB device will show up as a “Spectrum Digital XDS510 USB” under this class. You can view this information under Windows Device Manager. Connect the supplied USB cable to your XDS510 USB Galvanic JTAG emulator.

Figures 2-2 and 2-3 show two typical configurations in which the XDS510 USB Galvanic JTAG emulator can be used with a host PC and target board.





2.2.2 Setting Up and Running Code Composer Studio

To set up Code Composer Studio execute the following checklist:

- Select the Code Composer Setup Icon from the desktop.
- From the CC Setup you can either import a new configuration or select from an existing one. From the filters pane select the platform “**xds510usb**”. This will give you a list of predefined configurations for the XDS510USB emulator. If one of these configurations does not exactly match your target then select the closest configuration. You can modify this configuration to meet your needs. Setup changed dramatically between CCS 2.2x and 3.x so see your CCStudio documentation for more details.
- If you want to change the configuration of your setup simply right mouse click on the configuration under “**System Configuration**”, then select “**Properties**”. You can modify the individual properties for your setup. The I/O port under Board Properties should be set to 0x510 for the XDS510-USB emulator.
- Save your configuration and exit CC Setup.

- You can now start Code Composer Studio by double-clicking on the appropriate CCS icon. When CCS starts the XDS510-USB application loader will download the emulation driver application. Once the emulation application is loaded, the XDS510-USB emulator will enumerate and CCS will start. If there is a problem during the load or enumeration phase then the loader application will display an error/status message. Save your configuration and exit CC Setup.

- If you are running CCS 3.1, once CCS has started select **Debug->Connect** from the menu bar. Target **Connect/Disconnect** is a new feature in CCS 3.1, for more details go to your CCS online help. Save your configuration and exit CC Setup.

2.3 XDS510 USB Galvanic JTAG Emulator LED

The XDS510 USB Galvanic JTAG Emulator has one (1) red Light Emitting Diode (LED). This LED provides the user with the status of the emulator. The meaning of the LED is described in the table below.

Table 1: XDS510 USB Galvanic JTAG Emulator LEDs

LED Name	Function
USB ACTIVE	Indicates activity over the USB Bus

Chapter 3

Specifications For Your Target System's Connection to the Emulator

This chapter contains information about connecting your target system to the emulator. Your target system must use a special 14-pin connector for proper communication with the emulator.

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3.1 Designing Your Target System’s Emulator Connector (14-pin Header)

Certain devices support emulation through a dedicated emulation port. This port is a superset of the IEEE 1149.1 (JTAG) standard and is accessed by the emulator. To perform emulation with the emulator, your target system must have a 14-pin header (2 rows of 7 pins) with the connections that are shown in Figure 3-1. Table 1 describes the emulation signals.

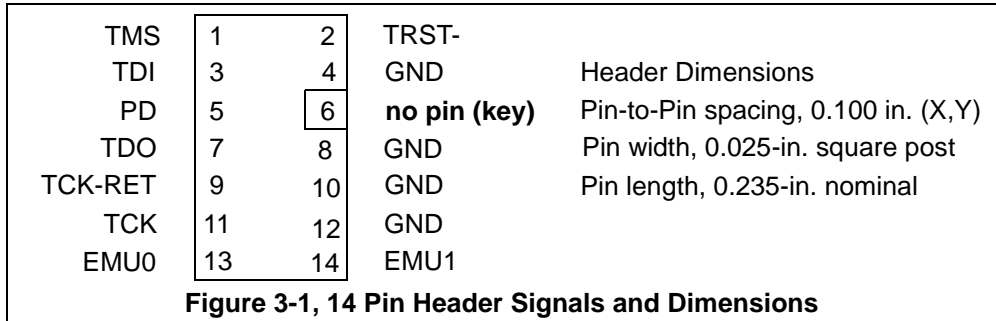


Table 1: 14-Pin Header Signal Description

Pin #	Signal	Description	Emulator State	Target State
1	TMS	JTAG test mode select.	Output	Input
3	TDI	JTAG test data input.	Output	Input
7	TDO	JTAG test data output.	Input	Output
11	TCK	JTAG test clock. TCK is a 12-MHz clock source from the emulation pod. This signal can be used to drive the system test clock.	Output	Input
2	TRST-	JTAG test reset.	Output	Input
13	EMU0	Emulation pin 0.	I/O	I/O
14	EMU1	Emulation pin 1.	I/O	I/O
5	PD	Presence detect. Indicates that the emulation cable is connected and that the target is powered up. PD should be tied to the target processor’s I/O pins Vcc. This pin draws up to 60 ma. current for target side emulation electronics.	Input	Output
9	TCK_RET	JTAG test clock return. Test clock input to the emulator. May be a buffered or unbuffered version of TCK.	Input	Output

Although you can use other headers, recommended parts include:

straight header, unshrouded	DuPont Connector Systems part # 67996-114
right-angle header, unshrouded	DuPont Connector Systems part # 68405-114

3.2 Bus Protocol

The IEEE 1149.1 specification covers the requirements for JTAG bus slave devices (such as the TMS320C5x family) and provides certain rules, summarized as follows:

- ___ The TMS/TDI inputs are sampled on the rising edge of the TCK signal of the device.

- ___ The TDO output is clocked from the falling edge of the TCK signal of the device

When JTAG devices are daisy-chained together, the TDO of one device has approximately a half TCK cycle set up to the next device's TDI signal. This type of timing scheme minimizes race conditions that would occur if both TDO and TDI were timed from the same TCK edge. The penalty for this timing scheme is a reduced TCK frequency.

The IEEE 1149.1 specification does not provide rules for JTAG bus master (emulator) devices.

3.3 Emulator Cable Pod Logic

Figure 3-2 shows a portion of the emulator cable pod. These are the functional features of the emulator pod:

- Signals TMS and TDI are generated from the rising edge of TCK_RET.
- Signals TMS, TDI, TCK, and TRST- are series-terminated to reduce signal reflections.
- A 12-MHz test clock source is provided. You may also provide your own test clock for greater flexibility.

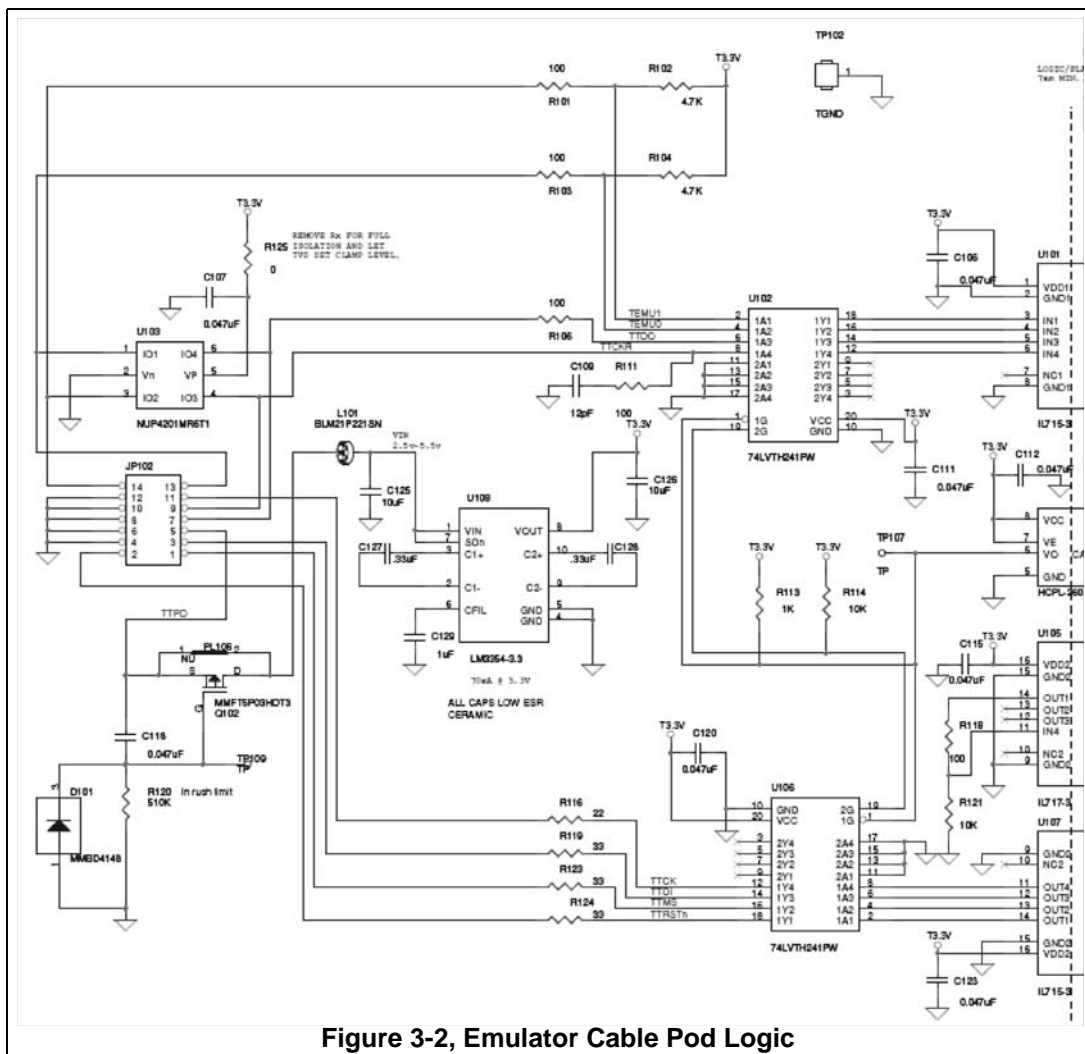


Figure 3-2, Emulator Cable Pod Logic

3.4 Target Power Requirements

The PD pin drives a Buck-Boost regulator to supply power for the target side JTAG electronics. The voltage and current requirements of the PD pin are shown below.

Table 2: Target Power Requirements

Signal	Requirements
PD Vin	+2.5V to +5.5V
PD Icc	60 mA max, 35mA typical at +3.3V, 12 Mhz TCK

3.5 Emulator Cable Pod Signal Timing

Figure 3-3 shows the signal timings for the emulator. Table 2 defines the timing parameters for the emulator. The timing parameters are calculated from standard data sheet parts used in the emulator and cable pod. These parameters are for reference only. Spectrum Digital does not test or guarantee these timings. The emulator pod uses TCK_RET as its clock source for internal synchronization. TCK is provided as an optional target system test clock source.

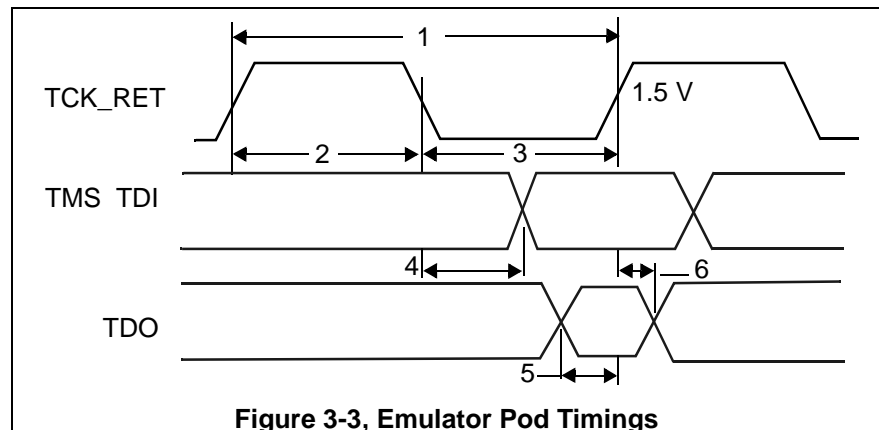


Figure 3-3, Emulator Pod Timings

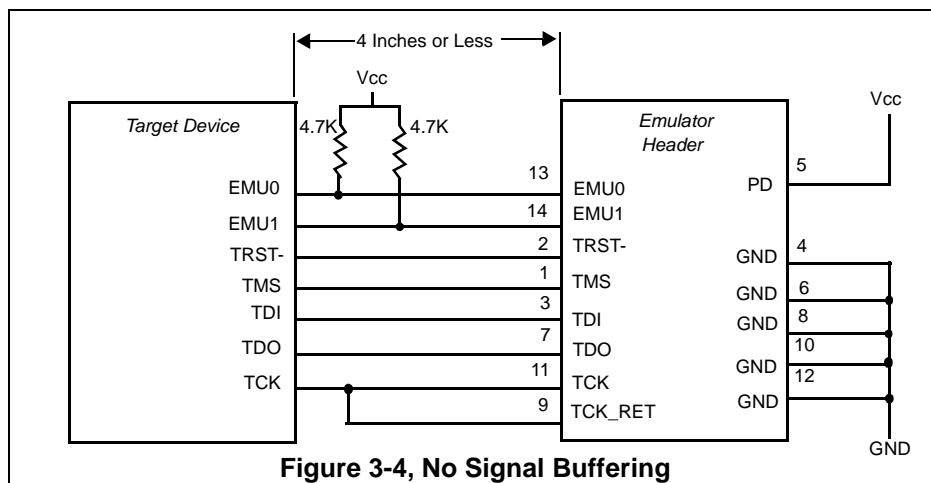
Table 3: Emulator Pod Timing Parameters

No	Reference	Description	Min	Max	Units
1	t_{TCKmin}	TCK_RET period	50	10000	ns
2	$t_{TCKhighmin}$	TCK_RET high pulse duration	15		ns
3	$t_{TCKlowmin}$	TCK_RET low pulse duration	15		ns
4	$td_{(XTMX)}$	TMS/TDI valid from TCK_RET low	5	22	ns
5	$tsu_{(XTDOmin)}$	TDO setup time to TCK_RET high	5		ns
6	$thd_{(XTDOmin)}$	TDO hold time from TCK_RET high	5		ns

3.6 Buffering Signals Between the Emulator and the Target System

It is extremely important to provide high-quality signals between the emulator and the target device on the target system. If the distance between the emulation header and the target device is greater than 6 inches, the emulation signals must be buffered. The need for signal buffering and placement of the emulation header can be divided into two categories:

- **No signal buffering.** As shown in figure 3-4, the distance between the header and the target device should be no more than 6 inches.



- **Buffered emulation signals.** Figure 3-5 shows the distance between the emulation header and the target device is greater than 6 inches. The target device signals--TMS, TDI, TDO, and TCK_RET are buffered through the same package.

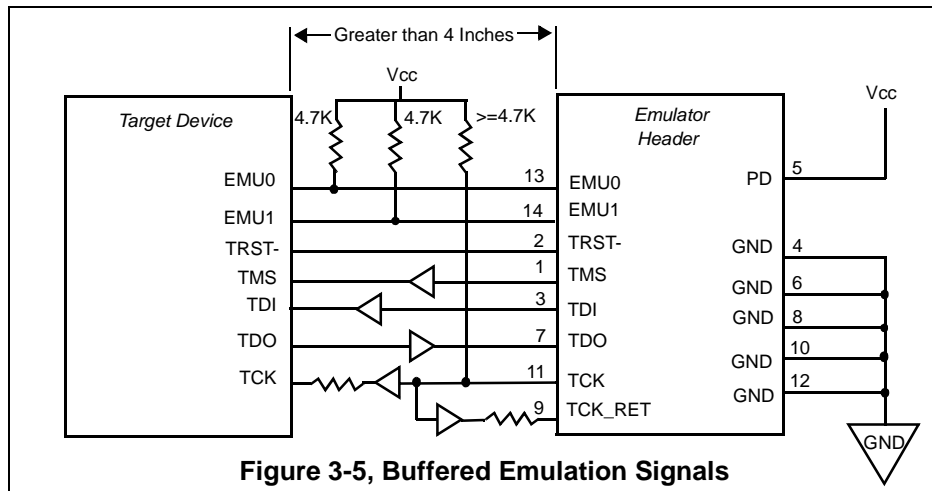


Figure 3-5, Buffered Emulation Signals

- The EMU0 and EMU1 signals must have pullups to Vcc. The pullup resistor value should be chosen to provide a signal rise time less than 10 uS. A 4.7k ohm resistor is suggested for most applications. EMU0-1 are I/O pins on the target device, however, they are only inputs to the emulator. In general, these pins are used in multiprocessor systems to provide global run/stop operations.
- It is extremely important to provide high quality signals, especially on the processor TCK and the emulator TCK_RET signal. In some cases, this may require you to provide special PWB trace routing and to use termination resistors to match the trace impedance. The emulator pod does provide fixed series termination on the TMS, TCK, and TDI signals.

Figure 3-6 shows an application with the system test clock generated in the target system. In this application the TCK signal is left unconnected.

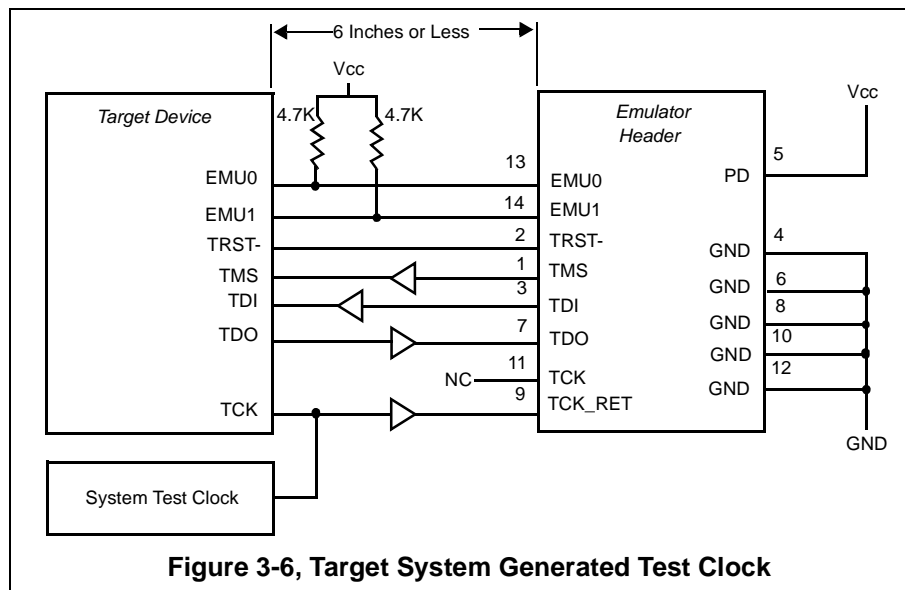


Figure 3-6, Target System Generated Test Clock

There are two benefits to having the target system generate the test clock:

- The emulator provides only a single 12-MHz test clock. If you generate your own test clock, you can set the frequency to match your system requirements.
- In some cases, you may have other devices in your system that require a test clock when the emulator is not connected.

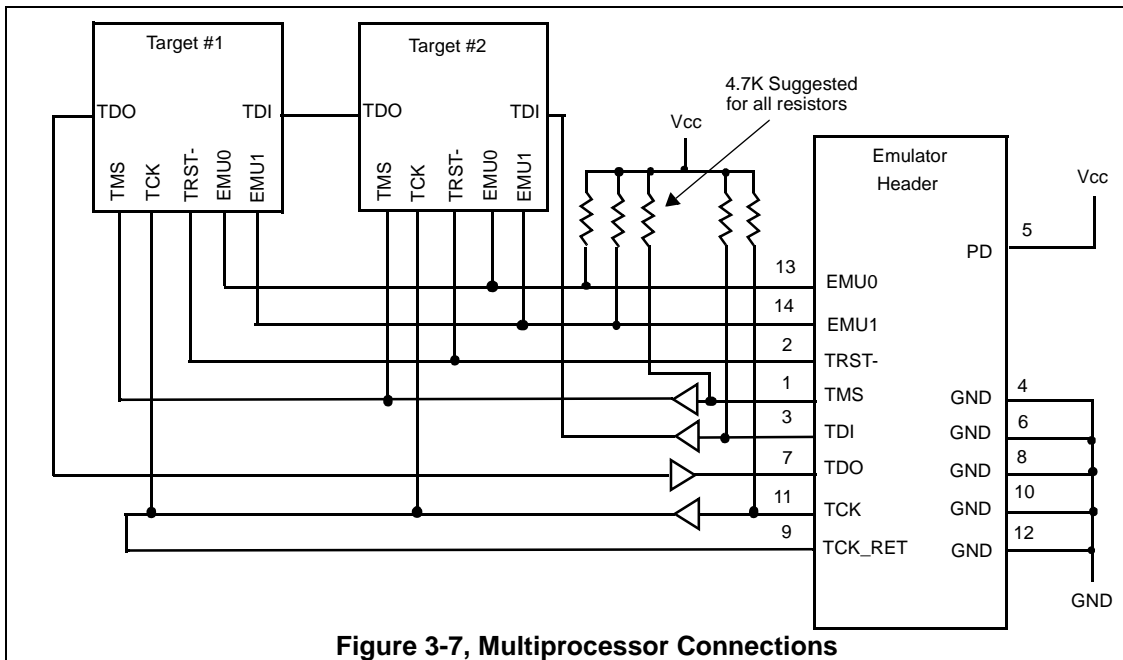


Figure 3-7, Multiprocessor Connections

Figure 3-7 shows a typical multiprocessor configuration. This is a daisy chained configuration (TDO-TDI daisy-chained), which meets the minimum requirements of the IEEE 1149.1 specification. The emulation signals in this example are buffered to isolate the processors from the emulator and provide adequate signal drive for the target system. One of the benefits of a JTAG test interface is that you can generally slow down the test clock to eliminate timing problems. Several key points to multiprocessor support are as follows:

- The processor TMS, TDI, TDO, and TCK should be buffered through the same physical package to better control timing skew.
- The input buffers for TMS, TDI, and TCK should have pullups to Vcc. This will hold these signals at a known value when the emulator is not connected. A pull up resistor of 4.7k ohms is suggested.

3.7 Emulation Timing Calculations

The following are a few examples on how to calculate the emulation timings in your system. For actual target timing parameters, see the appropriate device data sheets.

Assumptions:

$t_{su(TTMS)}$	Target TMS/TDI setup to TCK high	5 ns
$t_{h(TTMS)}$	Target TMS/TDI hold from TCK high	5 ns
$t_{d(TTDO)}$	Target TDO delay from TCK low	10 ns
$t_{d(bufmax)}$	Target buffer delay maximum	7 ns
$t_{d(bufmin)}$	Target buffer delay minimum	1 ns
$t_{(bufskew)}$	Target buffer skew between two devices in the same package: $[t_{d(bufmax)} - t_{d(bufmin)}] \times 0.15$.9 ns
$t_{tckfactor}$	Assume a 40/60 duty cycle clock	0.4

Given in Table 2:

$t_{d(XTMSmax)}$	Emulator TMS/TDI delay from TCK_RET high, max	22 ns
$t_{su(XTDOmin)}$	TDO setup time to emulator TCK_RET high	5 ns

There are two key timing paths to consider in the emulation design:

- the TCK_RET/TDI(t_{prdtck_TMS}) path, and
- the TCK_RET/TDO(t_{prdtck_TDO}) path.

In each case, the worst case path delay is calculated to determine the maximum system test clock frequency.

Case 1: Single processor, direct connection, TMS/TDI timed from TCK_RET.

$$\begin{aligned}t_{\text{prdtck_TMS}} &= (t_{\text{d(XTMSmax)}} + t_{\text{su(TTMS)}}) * 2 \\ &= (22\text{ns} + 5\text{ns}) * 2 \\ &= 54\text{ns} \text{ (18.5 MHz)}\end{aligned}$$

$$\begin{aligned}t_{\text{prdtck_TDO}} &= [t_{\text{d(TTDO)}} + t_{\text{su(XTDOmin)}}] / t_{\text{ckfactor}} \\ &= (10\text{ns} + 5\text{ns}) / 0.4 \\ &= 37.5\text{ns} \text{ (26.6 MHz)}\end{aligned}$$

In this case, the TCK/TMS-TDI path is the limiting factor.

Case 2: Single/multiple processor, TMS/TDI buffered input; TCK_RET/TDO buffered output, TMS/TDI timed from TCK_RET.

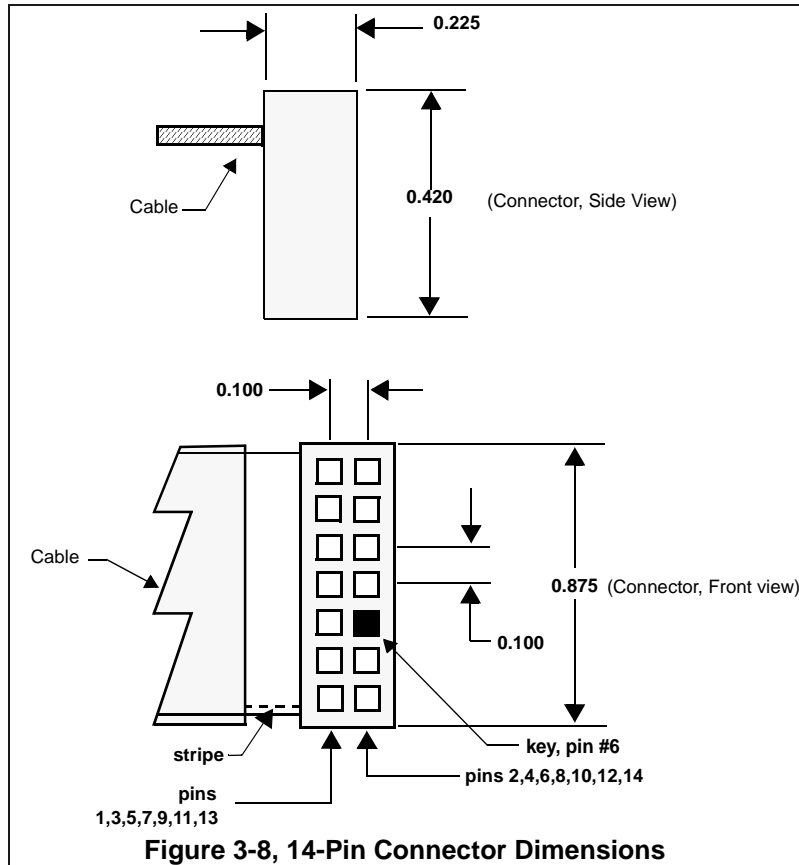
$$\begin{aligned}t_{\text{prdtck_TMS}} &= (t_{\text{d(XTMSmax)}} + t_{\text{su(TTMS)}} + 2t_{\text{d(bufmax)}}) * 2 \\ &= (22\text{ns} + 5\text{ns} + 2(7\text{ns})) * 2 \\ &= 82\text{ns} \text{ (12.2 MHz)}\end{aligned}$$

$$\begin{aligned}t_{\text{prdtck_TDO}} &= (t_{\text{d(TTDO)}} + t_{\text{su(XTDOmin)}} + t_{\text{bufskew}}) / t_{\text{ckfactor}} \\ &= (10\text{ns} + 5\text{ns} + 0.9 \text{ ns}) / 0.4 \\ &= 39.8\text{ns} \text{ (25.1 MHz)}\end{aligned}$$

In this case, the TCK/TMS-TDI path is the limiting factor.

3.8 14 Pin Target Connector

The tail of the emulator has a 14 (2x7) pin female header. The dimension of this header is shown below.



Note: All dimensions are in inches and are nominal dimensions, unless otherwise specified.

Appendix A

Mechanical Information

This appendix contains the mechanical information about the XDS510 USB Galvanic JTAG Emulator produced by Spectrum Digital.

B.1 Mechanical Dimensions of the XDS510 USB Galvanic JTAG Emulator

The XDS510 USB Galvanic JTAG Emulator consists of a 6-foot USB cable, the XDS510 USB Galvanic emulator pod, and a short section of cable (tail) that connects to the target system. The overall cable length is approximately 6 feet, 10 inches. Figure B-1 shows the mechanical dimensions for the XDS510 USB Galvanic JTAG emulator pod and short cable. The XDS510 USB Galvanic JTAG emulator enclosure is nonconductive plastic with one recessed metal screw.

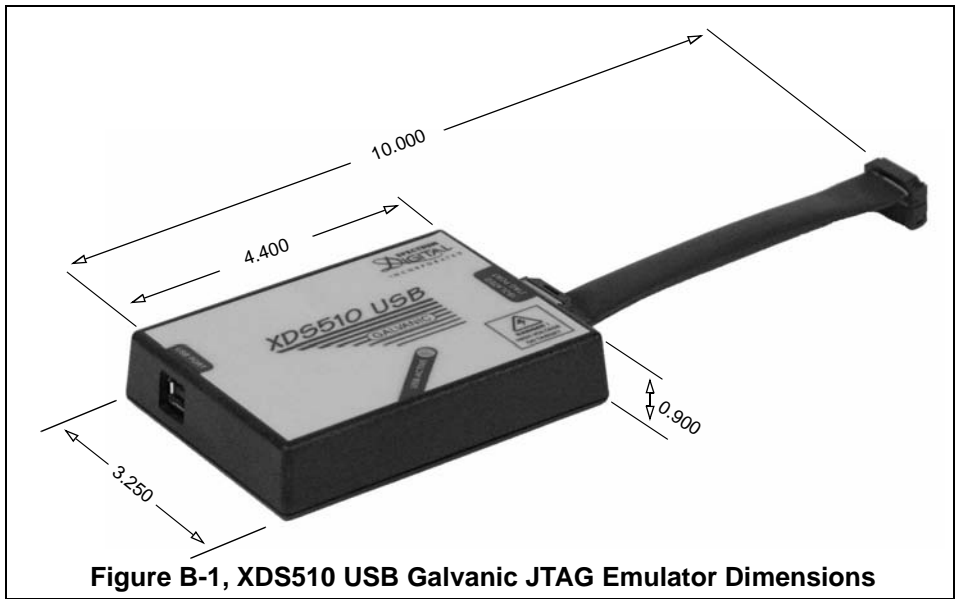


Figure B-1, XDS510 USB Galvanic JTAG Emulator Dimensions

Note: All dimensions are in inches and are nominal dimensions, unless otherwise specified.



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